JC05 Rec'd PCT/PTO 14 MAR 2002

dc-304666°FORM PTO-1390 TRADEMARK OFFICE (REV 11-2000) U S DEPARTMENT OF COMMERCE PATENT AND	ATTORNEY'S DOCKET NUMBER
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. § 371	449122024200
	U.S. APPLICATION NO. (If known, see 37 CFR 1.5) 10/070991 Not yet assigned

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE00/03109	September 7, 2000	September 14,1999

TITLE OF INVENTION

SERIAL DATA TRANSMISSION VIA A BUS SYSTEM

APPLICANT(S) FOR DO/EO/US

Michael DIEHL

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. ☒ The US has been elected by the expiration of 19 months from the priority date (PCT Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   - a. ☒ is attached hereto (required only if not communicated by the International Bureau).
   - b. ☒ has been communicated by the International Bureau.
   - c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ An English language translation of the International Application under PCT Article 19 (35 U.S.C. 371(c)(2)).
   - a. ☒ is attached hereto.
   - b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)).
   - a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   - b. ☐ have been communicated by the International Bureau.
   - c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   - d. ☐ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☒ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. ☒ Other items: 1) Application Data Sheet; 2) Int'l Search Report; 3) IPER; 4) Return receipt postcard.

CERTIFICATE OF HAND DELIVERY

I hereby certify that this correspondence is being hand filed with the United States Patent and Trademark Office in Washington, D.C. on March 13, 2002.

Melissa Garton

Melissa Garton

JC13 Rec'd PCT/PTO 14 MAR 2002

U.S. APPLICATION NO. (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY DOCKET NO.
Not yet assigned 10/070991	PCT/DE00/03109	449122024200

21. ☒ The following fees are submitted:

BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(5)):

Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO..........................$1,040.00

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO......................$890.00

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO...........................$740.00

International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provision of PCT Article 33(1)-(4) $710.00

International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) $100.00

				CALCULATIONS	PTO USE ONLY
			ENTER APPROPRIATE BASIC FEE AMOUNT =	$890.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).				$0	
CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	- 20 =		x $18.00	$0	
Independent claims	- 3 =		x $84.00	$0	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $280.00	$0	
			TOTAL OF ABOVE CALCULATIONS =	$890.00	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by ½.				$0	
			SUBTOTAL =	$890.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$0	
			TOTAL NATIONAL FEE =	$890.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00 per property** +				$40.00	
			TOTAL FEES ENCLOSED =	$930.00	
				Amount to be refunded:	$
				charged:	$

a. ☒ Please charge my **Deposit Account No. 03-1952** (referencing Docket No. 449122024200) in the amount of $930.00 to cover the above fees. A duplicate copy of this sheet is enclosed.

b. ☒ The Commissioner is hereby authorized to charge any additional fees that may be required, or credit any overpayment to **Deposit Account No. 03-1952** (referencing Docket No. 449122024200).

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Kevin R. Spivak
Morrison & Foerster LLP
2000 Pennsylvania Avenue, N.W.
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Kevin R. Spivak (signature)

SIGNATURE

Kevin R. Spivak
Registration No. 43,148

March 14, 2002

10/070991
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CERTIFICATE OF HAND DELIVERY

I hereby certify that this correspondence is being hand filed with the United States Patent and Trademark Office in Washington, D.C. on March 14, 2002.

Melissa Garton

Melissa Garton

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

Michael DIEHL

Serial No.: Not yet assigned

Filing Date: March 14, 2002

For: SERIAL DATA TRANSMISSION VIA A BUS SYSTEM

Examiner: Not yet assigned

Group Art Unit: Not yet assigned

PRELIMINARY AMENDMENT

BOX PCT
Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination on the merits, please amend this application as follows:

<u>In the Claims:</u>

Please cancel claims 1-21.

Please add new claims 22-42 as follows:

22. (New) A passive component for a bus system, comprising:

a bus interface to connect to a bus;

a serial interface to serially read out and read in data;

a data memory with an output area to store data read in via the bus interface and to be read out via the serial interface;

an input area to store data read in via the serial interface and to be read out via the bus interface;

a control device to control the transmission and storage of data; and

a detection device to detect the status of the output area and of the input area and provide corresponding status information, which status information is used as the basis for reading data into the output area and reading data out of the input area via the bus interface when the bus system is connected.

23. (New) The passive component as claimed in claim 1, further comprising a comparative device to periodically compare the status information with corresponding status information of an active component of a connected bus system, the control device controlling the reading in and reading out of data on the basis of the periodic comparison.

24. (New) The passive component as claimed in claim 2, a data packet is not read out of a corresponding output area of the active component and into the output area until the output area is ready to receive the data packet.

25. (New) The passive component as claimed in claim 3, further comprising a buffer to buff a data packet which is to be read out of the output area via the serial interface.

26. (New) The passive component as claimed in claim 3, wherein the data packet is not read into the input area via the serial interface until a corresponding input area of the active component is ready to receive the data packet.

27. (New) The passive component as claimed in claim 5, further comprising a buffer to buffer the data packet, to be read into the input area via the serial interface, if the input area of the active component is not yet ready to receive it.

28. (New) The passive component as claimed in claim 1, wherein the detection device comprises comprise an acknowledgement counter to count data packets which are read out via the serial interface, and a sequence counter to count data packets which are read in via the serial interface, the counting values serving as the status information.

29. (New) The passive component as claimed in claim 1, wherein a maximum size of the input area and of the output area can be set in a variable fashion, the data packets which are to be stored therein being able to have any desired sizes within the respectively set maximum size.

30. (New) An active component for exchanging data with a passive component, comprising:

a bus interface to connect a bus;

a data memory with an output area to store data in the output area of the passive component and to be read out via a serial interface;

an input area of data which is read out of the input area of the passive component;

a control device to control the transmission and the storage of data;

a detection device to detect the status of the output area and of the input area and provide status information, which status information is used by the active component, as the basis for reading data from the passive element into the input area via the bus interface and reading data out of the output area to the passive component.

31. (New) The active component as claimed in claim 9, further comprising a comparative device to periodically compare the status information with corresponding status information of the passive component, the control device controlling the reading in and reading out of the data on the basis of the periodic comparison.

32. (New) The active component as claimed in claim 9, further comprising a serial interface to serially read data into the output area and to serially read data out of the input area.

33. (New) The active component as claimed in claim 11, wherein a data packet is not read into the output area of the active component via the serial interface until the output area of the passive component is ready to receive the data packet.

34. (New) The active component as claimed in claim 11, wherein a data packet to be read out via the serial interface is not read from the input area of the passive component into the input area of the active component until the input area of the active component is ready to receive the data packet.

35. (New) The active component as claimed in claim 9, wherein the detection device comprises an acknowledgement counter to count data packets which are read out via the serial interface, and a sequence counter to count data packets which are read in via the serial interface, the counting values serving as the status information.

36. (New) The active component as claimed in claim 9, wherein a maximum size of the input area and of the output area can be set in a variable fashion, the data packets which are to be stored therein being able to have any desired size within the respectively set maximum size.

37. (New) A method for reading serial data into and out of a bus system which comprises a passive component, forming a slave station, with a serial interface and a data memory, which has an output area for reading out data via the serial interface and comprises an input area, and an active component, forming a master station, with a data memory which has an output area and an input area, comprising:

transferring data at the request of the active component via the passive component; and

detecting the status of the output areas and of the input areas and providing status information corresponding to the status, which status information is used as the basis for the transfer of the data of the output area of the active component into the output area of the passive component, and the transfer of the data of the input area of the passive component into the input area of the active component.

38. (New) The method as claimed in claim 16, further comprising comparing the status information of the output areas of the active and passive components and periodically comparing the status information of the input areas of the active and passive components, and reconciliation of the output areas and the input areas carried out on the basis of comparison.

39. (New) The method as claimed in claim 16, wherein a data packet is not read into the output area of the active component until the output area of the passive component is ready to receive the data packet.

40. (New) The method as claimed in claim 16, wherein a data packet is not read from the input area of the passive component into the input area of the active component until the input area of the active component is ready to receive the data packet.

41. (New) The method as claimed in claim 18, wherein the read-out data packets and the read-in data packets are counted, the counting values serving as the status information.

42. (New) The method as claimed in claim 18, wherein a maximum size of the input areas and of the output areas can be set in a variable fashion, the data packets to be stored therein being able to have any desired size within the respectively set maximum size.

In the Abstract:

Please replace the Abstract with the substitute Abstract attached hereto.

REMARKS

Amendments to the specification have been made and are submitted herewith in the attached Substitute Specification. We have included both a clean copy of the specification and a marked-up version showing the changes made. The claims and abstract have been amended herewith in the Preliminary Amendment. All amendments have been made to place the application in proper U.S. format and to conform with proper grammatical and idiomatic English. None of the amendments herein are made for reasons related to patentability. No new matter has been added.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**".

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. 449122024200. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Respectfully submitted,

Dated: March 14, 2002

Kevin R. Spivak
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25. (New) The passive component as claimed in claim 3, further comprising a buffer to buff a data packet which is to be read out of the output area via the serial interface.

26. (New) The passive component as claimed in claim 3, wherein the data packet is not read into the input area via the serial interface until a corresponding input area of the active component is ready to receive the data packet.

27. (New) The passive component as claimed in claim 5, further comprising a buffer to buffer the data packet, to be read into the input area via the serial interface, if the input area of the active component is not yet ready to receive it.

28. (New) The passive component as claimed in claim 1, wherein the detection device comprises comprise an acknowledgement counter to count data packets which are read out via the serial interface, and a sequence counter to count data packets which are read in via the serial interface, the counting values serving as the status information.

29. (New) The passive component as claimed in claim 1, wherein a maximum size of the input area and of the output area can be set in a variable fashion, the data packets which are to be stored therein being able to have any desired sizes within the respectively set maximum size.

30. (New) An active component for exchanging data with a passive component, comprising:

a bus interface to connect a bus;

a data memory with an output area to store data in the output area of the passive component and to be read out via a serial interface;

an input area of data which is read out of the input area of the passive component;

a control device to control the transmission and the storage of data;

a detection device to detect the status of the output area and of the input area and provide status information, which status information is used by the active component, as the basis for reading data from the passive element into the input area via the bus interface and reading data out of the output area to the passive component.

31. (New) The active component as claimed in claim 9, further comprising a comparative device to periodically compare the status information with corresponding status information of the passive component, the control device controlling the reading in and reading out of the data on the basis of the periodic comparison.

32. (New) The active component as claimed in claim 9, further comprising a serial interface to serially read data into the output area and to serially read data out of the input area.

33. (New) The active component as claimed in claim 11, wherein a data packet is not read into the output area of the active component via the serial interface until the output area of the passive component is ready to receive the data packet.

34. (New) The active component as claimed in claim 11, wherein a data packet to be read out via the serial interface is not read from the input area of the passive component into the input area of the active component until the input area of the active component is ready to receive the data packet.

35. (New) The active component as claimed in claim 9, wherein the detection device comprises an acknowledgement counter to count data packets which are read out via the serial interface, and a sequence counter to count data packets which are read in via the serial interface, the counting values serving as the status information.

36. (New) The active component as claimed in claim 9, wherein a maximum size of the input area and of the output area can be set in a variable fashion, the data packets which are to be stored therein being able to have any desired size within the respectively set maximum size.

37. (New) A method for reading serial data into and out of a bus system which comprises a passive component, forming a slave station, with a serial interface and a data memory, which has an output area for reading out data via the serial interface and comprises an input area, and an active component, forming a master station, with a data memory which has an output area and an input area, comprising:

transferring data at the request of the active component via the passive component; and

detecting the status of the output areas and of the input areas and providing status information corresponding to the status, which status information is used as the basis for the transfer of the data of the output area of the active component into the output area of the passive component, and the transfer of the data of the input area of the passive component into the input area of the active component.

38. (New) The method as claimed in claim 16, further comprising comparing the status information of the output areas of the active and passive components and periodically comparing the status information of the input areas of the active and passive components, and reconciliation of the output areas and the input areas carried out on the basis of comparison.

39. (New) The method as claimed in claim 16, wherein a data packet is not read into the output area of the active component until the output area of the passive component is ready to receive the data packet.

40. (New) The method as claimed in claim 16, wherein a data packet is not read from the input area of the passive component into the input area of the active component until the input area of the active component is ready to receive the data packet.

41. (New) The method as claimed in claim 18, wherein the read-out data packets and the read-in data packets are counted, the counting values serving as the status information.

42. (New) The method as claimed in claim 18, wherein a maximum size of the input areas and of the output areas can be set in a variable fashion, the data packets to be stored therein being able to have any desired size within the respectively set maximum size.

In the Abstract:

Please replace the Abstract with the substitute Abstract attached hereto.

SERIAL DATA TRANSMISSION VIA A BUS SYSTEM

Abstract

The present invention relates to a passive component for a bus system, such as, for example, a field bus system, having a bus interface for connection to a bus, a serial interface for serially reading out and reading in data, a data memory with an output area for storing data which has been read in via the bus interface and is to be read out via the serial interface and an input area for storing data which has been read in via the serial interface and is to be read out via the bus interface, and a control device for controlling the transmission and storage of data, a detection device to detect the status of the output area and of the input area and providing corresponding status information being provided, which status information is used as the basis for reading data into the output area and reading data out of the input area via the bus interface when the bus system is connected. The present invention also comprises a corresponding active component for exchanging data with such passive component, and a method for reading data in and out of a bus system which comprises such a passive component and such an active component. The present invention makes data communication possible between such a bus system and one or more decentralized peripherals or serial interfaces.

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Docket No. 449122024200

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Description

Serial data transmission via a bus system

The present invention relates to the transmission of serial data via a bus system, in particular the transmission of serial data via a V.24 interface via a field bus, for example the PROFIBUS DP. In particular, the present invention relates to a passive component and an active component for the bus system, at least the passive component having a serial interface for the reading in and reading out of data. Furthermore, the present invention relates to a method for the reading in and reading out of serial data via a bus system.

Bus systems are in use in a wide variety of technical applications. In particular field buses, for example the PROFIBUS (PROcesFieldBUS) according to DIN 19245 (EN 50170 since 1996) are widely used, for example, in automation technology, for the transmission of data over relatively long paths. In contrast to most systems which transmit data in a parallel fashion, the PROFIBUS is a serial bus system in which data is transmitted serially. Field buses have wide-ranging fields of application because they can be connected to, and operated with, both simple and complex components (stations). Furthermore, they are advantageous in terms of the low connection costs and reduced expenditure on cabling. Additional advantages are short reaction times and simple protocols which make field busses real-time-capable. Other factors to note are the high degree of immunity to faults, even over large distances, simple integration in the existance of the systems and the ease with which the respective elements are made independently irreplaceable.

An example of such a field bus is the PROFIBUS according to DIN 19245, which can be divided into various hierarchical layers on the basis of different

functionalities and modes of operation. Part 1 of DIN 19245 in this case defines the PROFIBUS layers 1 and 2, where the fieldbus datalink (FDL) is defined, for example. An example of the bus system of these layers is illustrated in Fig. 1. Part 2 of DIN 19245 defines the PROFIBUS layer 7 and contains the fieldbus message specification (FMS). Part 3 of DIN 19245 defines the PROFIBUS DP (decentralized peripherals) which comprises the PROFIBUS FDL of layers 1 and 2 and defines service interfaces and data interfaces for exchanging data with external peripheral data.

A fieldbus such as the PROFIBUS DP usually comprises one or more active stations and a plurality of passive stations. The active and passive stations or components are configured here in a master-slave relationship. This means that the active components actuate the passive components and/or read data in and out. The passive components operate only after being actuated by the active components. The problem with such fieldbusses is the reading out of the current data to external peripherals, such as for example computers. Existing systems are slow, inefficient and complicated.

The object of the present invention is thus to provide a passive component for a bus system, an active component for a bus system and a method for reading data in and out of a bus system which permit rapid, efficient and reliable reading out and reading in of data to or from one or more of the central peripherals.

This object is achieved by means of a passive component for a bus system as claimed in claim 1, comprising having a bus interface for connection to a bus, a serial interface for serially reading out and reading in data, a data memory with an output area to the memory of data which has been read in via the

bus interface and is to be read out via the serial interface, and an input area for storing data which has been read in via the serial interface and is to be read out via the bus interface, and a control device for controlling the transmission and storage of data, detection means for detecting the status of the output area and of the input area and providing corresponding status information being provided, which status information is used as the basis for reading data in via the output area and reading data out of the input area via the bus interface when the bus systems are connected.

The object above is also achieved by means of an active component for exchanging data with such a passive component as claimed in claim 9, having a bus interface for connection to a bus, a data memory with an output area for storing data which is to be stored in the output area of the passive component and is to be read out via its serial interface, and an input area of data which is read out of the input area of the passive component, and a control device for controlling the transmission and storage of data, detection means for detecting the status of the output area and of the input area and for providing corresponding status information being provided, which status information is used by the active component as the basis for reading data from the passive component into the input area via the bus interface and for transmitting data from the output area to the passive component.

The object above is also achieved by means of a method for reading serial data into and out of a bus system as claimed in claim 16, the bus system comprising a passive component with a serial interface and a data memory which has an output area for reading out data via the serial interface and an input area, and comprises an active component with

a data memory which has an output area and an input area, the statuses of the output areas and of the input areas being detected and corresponding status information being provided, which is used as the basis for the reconciliation of the output area of the active component and the output area of the passive component, and of the input area of the passive component and the input area of the active component.

The passive component according to the present invention advantageously has a comparative means for periodically comparing the status information with corresponding status information of the active component, the control device controlling the reading in and reading out of data on the basis of this periodical comparison. For example, in the abovementioned PROFIBUS DP system, in which the output areas and input areas of the active and passive components are reconciled cyclically, the input areas and output areas of the passive component according to the present invention, and the input areas and output areas of the active component according to the present invention are reconciled, that is to say the data are copied, only if the status information indicates that the respective area has the corresponding predefined status which permits or requires the reconciliation of the data. For example, a data packet is not read out of the output area of the active component and into the output area of the passive component until the output area of the passive component is ready to receive this data packet. This means that first the respective data packet has to be read out of the output area of the passive component via the serial interface to a decentralized peripheral before a new data packet can be received. In this context, a buffer for buffering a data packet which is to be read out of the output area

via the serial interface can be provided in the passive component in order to enable the

output area of the passive component to be made vacant as quickly as possible so that a new data packet from the active component can be read in.

A data packet is furthermore advantageously not read into the input area of the passive component via the serial interface until the corresponding input area of the active component is ready to receive this data packet. In this case, too, it is possible to provide a buffer which buffers a data packet, to be read into the input area via the serial interface, if the input area of the active component is not yet ready to receive it.

The detection means for detecting the status of the output area and of the input area of the passive component advantageously comprise an acknowledgement counter for counting data packets which are read out via the serial interface of the passive component, and a sequence counter for counting data packets which are read in via the serial interface of the passive component, the counting values serving as the status information.

Furthermore, in the passive component according to the present invention, the maximum size of the input area and that of the output area can be set in a variable fashion, the data packets which are to be stored therein being able to have any desired size within the respectively set maximum size. As a result, a very flexible transmission of serial data in the bus system becomes possible.

The passive component described above and in accordance with the present invention is exclusively configured for the reading in and reading out of serial data via a corresponding serial interface, for example a V.24 interface. The active component according to the

present invention in this case controls this reading in and reading out of data via the

serial interface of the passive component. The data memory of the active component has an output area which is reconciled with the output area of the passive component according to the present invention, and also has an input area which is reconciled with the input area of the passive component according to the present invention. The active component according to the present invention can also have its own serial interface, for example a V.24 interface, for the serial reading of data into the corresponding output area for the serial reading of data out of the corresponding input area. Here, the data packet cannot be read into the output area of the active component via the serial interface until the output area of the passive component is ready to receive this data packet. On the other hand, a data packet which is to be read out via the serial interface of the active component cannot be read from the input area of the passive component into the input area of the active component until the input area of the active component is ready to receive this data packet. Similarly to the passive component, with the active component according to the present invention it is also advantageous if the detection means for detecting the status of the output area and of the input area comprise an acknowledgement counter for counting data packets read out via the serial interface, and a sequence counter for counting data packets read in via the serial interface, the target values serving as the status information. In the active element too, the maximum size of the input area and that of the output area can be set in a variable fashion, the data packets to be stored therein being able to have any desired size within the respectively set maximum size. The respective input area and the respective output area can have different sizes here. The size of the input areas and of the

output areas are also predefined here for the passive component by the active component.

The present invention is explained in more detail below by means of a preferred exemplary embodiment and with reference to the appended drawings, in which

Fig. 1 shows a schematic view of a bus system on which the present invention can be applied,

Fig. 2 shows a schematic view of a bus system with higher-value services than the bus system shown in Fig. 1 which forms the basis for the present invention, and

Fig. 3 shows a schematic view of an active component and of a passive component according to the present invention.

The PROFIBUS FDL system (shown in Fig. 1) of the layers 1 and 2 comprises a line-like bus structure in which active components (stations) 1a, 1b and 1c with the addresses 1, 8 and 25 are connected to a bus 4 via spur lines. The bus 4 has a line shape and is terminated at both ends by a bus termination 4. Passive components (stations) 2a, 2b, 2c and 2d with the addresses 3, 4, 9 and 39 are also connected to the bus 4 by spur lines. The address data items are of course examples.

The overall length of the bus 4 can be up to 1.2 km, while the spur lines to the active and passive components are 0.3 m long at maximum. The overall number of subscribers, i.e. the overall number of active and passive components is restricted to a maximum of 126. The active components 1a, 1b and 1c are connected by a logic token ring, that is to say a decentralized bus access takes place in accordance with the token passing principle. A central bus access is subordinated to this

superordinate decentralized passive access in accordance with the master-slave principle. The active components 1a, 1b and 1c are the master stations and form the logic token ring. Each component which has the token can carry out corresponding useful data services. The passive components 2a, 2b, 2c and 2d are slave stations which react to the access by the active components. The active components change data with one another, and the respective active station which is in possession of the token can actuate the other active and passive components. The passive components transmit and receive data only at the request of the active stations and do not participate in the active bus operation.

Each active component and each passive component has an electrical bus interface via which data is exchanged with other components. In the case of the PROFIBUS FDL as well as in the case of the PROFIBUS DP, for example RS 485 interfaces are used which permit data communication with a plurality of other components on the basis of 11 bit/characters (startbit/stop-bit/paritybis, 8 useful data bits).

Figure 2 shows an example of a PROFIBUS DP Monomaster system with an active component 1 (DP Master/Class 1) and a plurality of passive components 2a, 2b, 2c and 2d (DP slaves A, B, C and D) according to the present invention. The PROFIBUS DP comprises services of the PROFIBUS FDL which are described with respect to the in Fig. 1 and also defines higher-value services, namely service interfaces or data interfaces for communicating with their decentralized peripherals, as shown in Fig. 2. These functionalities of the active component 1 in the PROFIBUS DP system comprise here the data transfer via a data interface 5, via input data areas (input data) 6 and output data areas (output data) 7, and also configuration, stages detection and diagnostics. The passive stations 2a, 2b, 2c and

2d each have an input area (input) and an output area (output). The passive component 2a comprises here an input area 8a and an output area 9a, the passive component 2b comprises an input area 8b and an output area 9b, the passive component 2c comprises an input area 8c and an output area 9c and the passive component 2d comprises an input area 8d and an output area 9d. All the passive components 2a, 2b, 2c and 2d are connected to the linear bus 4 via short spur lines, as is the active component 1. A large data memory is provided in the active component 1 and in it in each case the input areas and output areas of the passive components are mirrored, that is to say are present in identical forms. For this purpose, the active component 1 updates its input areas 6 and output areas 7 cyclically with those of the passive components. The output areas 9a, 9b, 9c and 9d of the passive components contain here the data which is to be read out from the passive components to respectively decentralized peripherals, and the input areas 8a, 8b, 8c and 8d contain the data which is to be read from respective decentralized peripherals into the passive components. The input area 6 of the active component 1 contains data to be read out from the active component 1 to a decentralized peripheral, while the output area 7 of the active component 1 contains data which is to be read in from such a decentralized peripheral.

Fig. 3 is a schematic illustration of an active component 10 according to the present invention and of a passive component 11 according to the present invention. The active component 10 and the passive component 11 as illustrated in Fig. 3 can be integrated, for example, as an active component 1 or passive component 2a, 2b, 2c or 2d into the bus systems shown in Figs. 1 and 2.

The passive component 11 which is shown in Fig. 3 comprises a bus interface 21 for connecting the passive component 11 to a bus, such as for example a field bus, as has been described above. Furthermore, the passive component comprises a serial interface 22, for example a V.24 interface for serially reading in and reading out data into and out of a peripheral, such as for example a computer. Furthermore, a data memory 24 with an output area 25 for storing data which has been read out via the bus interface 21 and is to be read in via the serial interface 22, and an input area 26 for storing data which has been read in via the serial interface 22 and is to be read out via the bus interface 21 is provided. The transmission and storage of data is controlled by a control device 23, an acknowledgement counter 27 for counting data packets which are read out via the serial interface 22, and a sequence counter 28 for counting data packets which are read in via the serial interface 22 being provided. The respective counting values serve as the status information with respect to the data packets stored in the output area 25 and input area 26. The acknowledgement counter 27 is embodied as part of the output area 25, while the sequence counter 28 is embodied as part of the input area 26. The data memory 24, which comprises the output area 25 and the input area 26, is, for example, a RAM (Random Access Memory). The control device 23 of the passive component 11 comprises a comparative means 29 for periodically comparing the status information with corresponding status information of the active element 10, the control device 23 controlling the reading in and reading out of data via the output area 25 and the input area 26 on the basis of this periodic comparison. An optional buffer 30 for buffering data packets which are to be read out of the output area via the serial interface 22 is provided between the control device 23 and the serial interface 22. The buffer 30 is also used for buffering a data packet which is to be read into the input area 26 via the serial

interface 22. The maximum size of the input area 26 and of the output area 25 of the passive component 11 can be set in a variable fashion, the data packets which are to be stored therein being able to have any desired size within the respectively set maximum size, as is explained in detail below.

The passive component 11 which is illustrated in Fig. 3 is connected to a correspondingly assigned active element 10 via its bus interface 21 with a bus system, for example a field bus such as the PROFIBUS DP. The active element 10 correspondingly comprises a bus interface 13 with which it is connected to the bus system. In addition, the active component comprises a data memory 15, for example a RAM, with an output area 16 for storing data which is to be stored in the output area 25 of the passive element 11 and data which is to be read out via its serial interface 22, and an input area 17 of data which has been read out of the input area 26 of the passive component 11. As has been explained above, the data of the output area 16 of the active component 10 and of the output area 25 of the passive component 11 is cyclically mirrored and/or reconciled, like the data of the input area 17 of the active component 10 and the data of the input area 26 of the passive component 11. Here, the data of the output area 16 of the active component 10 is transferred in the output area 25 of the passive component 11, and the data of the input area 26 of the passive component 11 is transferred into the input area 17 of the active component 10. The active component 10 also comprises an optional serial interface 12 for serially reading data into the output area 16 and for serially reading data out of the input area 17. In addition, an acknowledgement counter 19 for counting data packets which have been read out via the serial interface 12, and a sequence counter 19 for counting data packets which have been read out via the serial interface 12

and a sequence counter 18 for counting data packets which have been read in via the serial interface 12 are provided, the counting values serving as the status information, which is used as the basis for the reading of data from the passive component 11 into the input area 17 via the bus interface 13 and for the reading of data out of the output area 18 to the passive component 11. The transmission of data is controlled here by the control device 14 which comprises a comparative means 20 for periodically comparing the status information with corresponding status information of the passive component 11, the control device 14 controlling the reading in and reading out of data on the basis of this periodical comparison. The acknowledgement counter 19 is embodied as part of the input area 17, and the sequence counter 18 is embodied as part of the output area 16.

Like the input area 26 and the output area 25 of the passive component 11, the input area 17 and the output area 16 of the active component 10 can also be set with respect to the maximum size, the data packets which are to be stored in them being able to have any desired size within the respectively set maximum size. The maximum size of the input areas 17 and 26 and of the output areas 16 and 25 is set by the active component 10 when the bus system is initialized. For this purpose, the active component 10 sets up the data communication to the passive component 11 in accordance with EN 50 170 and DIN 19 245 when operation is started and transmits a diagnostic message to the passive component 11. The passive component 11, i.e. the control device 23 receives the diagnostic message and signals the corresponding diagnostic parameters back to the active component 10, i.e. its control device 14. The control device 14 of the active component 10 then transmits the parameters to be set to the control device 23 of the passive component 11, as a result of which the latter is parameterized and configured. The

setting of the parameters is correspondingly acknowledged by the passive element 11, in response to which the active component 10 transmits a configuration message to the passive component 11. From the configuration message, the passive component 11 detects the data area size for the input area 26 and the output area 25 and sets their sizes correspondingly. The sizes can be defined here in, for example, the limits 7 bytes to 244 bytes. The data area sizes which are set are then acknowledged by the passive component 11. During the further course of the operation, the data is cyclically updated in the input areas 17 and 26 and the output areas 16 and 25. The abovementioned variable setting of the sizes of the output areas and of the input areas is supported in a corresponding way by corresponding algorithms in the control devices 14 and 23.

It is to be emphasized that the passive component 11 according to the present invention is used exclusively for data communication between the bus system and one or more peripherals by means of the serial interface 22 and does not have any further functions. However, it is also conceivable for the active component 11 according to the present invention to perform additional control or sensor functions in the bus system. In all cases the data which is to be read out of the output area 16 of the active component 10 to the output area 25 of the passive component 11 and then via the serial interface 22 of the passive component 11 generally constitutes data which is used to actuate passive components of the bus system which perform control, sensor and actuator functions and the like. The data which has been read via the serial interface 22 of the passive component into the input area 26 and from there into the input area 17 of the active component 11 constitutes data which comprises the messages of the corresponding peripheral, connected to the serial interface 22, to the active component 10, these messages being able to be used in turn

for actuating other passive components of the bus system, for example.

In the passive component 11 according to the present invention, the data which is used within the bus system is thus converted into output data which is read out via the serial interface 22 to one or more decentralized peripherals, the serial interface 22 being able to be, for example, a V.24 or a RS 232 interface. On the other hand, the passive component 11 according to the present invention of one or more decentralized peripherals into the bus system converts data from serial data into data which has the data format necessary for the bus system.

In order to be able to transmit data between the bus system and one or more decentralized peripherals via the serial interface 22 of the passive component 11 or via the serial interface 12 of the active component 10, according to the present invention a further communications protocol, which is defined for example as in the following tables 1 and 2 is superimposed on the input areas 17 and 25 and the output areas 16 and 24. The serial interfaces 12 and 22 are given in this example as V.24 interfaces.

Table 1 presents the communications protocol for the output areas 16 and 24, that is to say the data transmission device from the active component to the passive component 11 for reading out the data via the serial interface 22 (V.24 interface) of the passive component 11.

Byte No.	**Designation**	**Function**
o-1	tx_seq	Sequence counter transmission of a V.24 telegram
o-2	rx_seq_ack	Acknowledgement counter for reception of a V.24 telegram
o-3	Command	Bit 0 0 no significance 1 reset of reception buffer DP slave before the

		new telegram is transmitted Bits 1..7 reserved
o-40	Reserved	00
o-5	rx_pref_len	Preset maximum byte number of a received telegram, if the value 00 is entered here the reception length is independently determined by the DP slave.
o-6	tx_len	Length data [byte] of telegram to be transmitted
o-7	Data 1	First octet to be transmitted via V.24
o-8	Data 2	Second octet to be transmitted via V.24
	Data...	...
o-(txlen + 6)	Data [tx_len]	Last octet to be transmitted via V.24

Table 2 represents the communications protocol for the input areas 17 and 26, i.e. the data transmission device from the passive component 11 to the active component 10 for data packets (telegrams) which have been received via the serial interface 22 (V.24 interface) of the passive component 11.

Byte No.	**Designation**	**Function**
i-1	tx_seq_ack	Acknowledgement counter for transmit data V.24
i-2	rx_seq	Sequence counter for reception of a V.24 telegram
i-3	rx_tx_fail	Fault message DP-slave, for format see below.
i-4	Reserved	00
i-5	Reserved	00
i-6	rx_len	Length data [byte] of the received telegram, the maximum length given in the range o-5 is not exceeded (provided <>0).
i-7	Data 1	Received data 1
i-8	Data 2	Received data 2
:	:	:
i-rx_len+6	Data [rx_len]	Last octet received data

The reception buffer of the passive component 11 is the buffer 30 for buffering data packets which are to be read in or read out.

The following table 3 represents an example of the display of fault messages of the passive component 11 in the component i-3 of the communications protocol for the input areas.

Bit position	Significance
0	Reception buffer overflow
1	Reception error, frame error
2	parity error
3	Other reception errors
4	Reserved (=0)
5	Reserved (=0)
6	Reserved (=0)
7	Internal PROFIBUS DP-slave error

If there is error-free transmission, i.e. error-free reading in of data via the serial interface 22 into the reception memory or buffer (reception buffer) 30 into the input area 26, the byte i-3 is equal to 0. In the case of an error, i.e. if i-3 is unequal to 0, the received data are nevertheless to be read into the input area 26 via the buffer 30 and thus read into the input area 17 of the active component 11 by means of the cyclical reading out via the bus system.

The principle of the transmission mechanism for transmitting data packets data packets to be out of the output area 16 and into the output area 25 and via the serial interface 22 to one or more peripherals will be explained below. The transmission mechanism is based here on a comparison of the bytes o-1 and i-1 of the transmission protocols such as are illustrated, for example, in tables 1 and 2,

in the comparator device 20 of the control device 14 of the active component 10 and the comparative device 29 of the control device 23 of the passive component 11. This means that the status or the current counter reading of the sequence counter 18 of the output area 16 and of the acknowledgement counter 27 of the output area 25 are compared. The two counter readings are each contained in byte o-1 and i-1. In principle, a data packet is not read out of the output area 16 of the active component 10 and into the output area 25 of the passive component 11 until the output area 25 is ready to receive this data packet, i.e. the output area 25 is empty. In order to speed up the reading of data packets out of the output area 16 of the active component 10 and into the output area 25 of the passive component 11, the data which is to be read out of the output area 25 via the serial interface 22 is buffered in the buffer 30.

When the data is read out, the control device 14 of the active component 10 firstly checks the bytes o-1 and i-1 for identity. Given identity, data packets which are to be read out can be entered into the output memory 16 of the active component 10 and the data is then, in cyclical reading out, copied into the output area 25 of the passive component 11, from which it is then read out via the serial interface 22. Given non-identity between the bytes o-1 and i-1, the transmission mechanism is still occupied, i.e. the reading of data out of the output area 25 via the serial interface 22 is not yet terminated so that no new data packets are allowed to be entered into the output area 16 of the active component 10. Given identity between the two bytes, data packets which are to be read out are thus entered into the output area 16 of the active component 10 starting from the byte o-7. The overall length of the data is entered in the byte o-6. The byte o-1 is then incremented by the value +1, as a result of which the bytes o-1 and i-1 are differentiated. As long as

this difference exists, no new data is allowed to be entered into the output area 16 of the active component 10.

The passive component 11, i.e. the comparator device 29 of the control device 23 also compares the bytes o-1 and i-1 and, when a difference is detected between these two bytes, it transmits output data from the output area 25 to the serial interface 22 via the buffer 30. When the reading-out operation from the output area 25 is terminated, the byte i-1 is incremented by the value +1, so that the byes i-1 and o-1 again have the same value, with the result that new data packets can be read into the output area 16 of the active component 10.

The reception mechanism for receiving data via the serial interface 22 of the passive component 11 is equivalent. Here, the bytes i-2 and o-2 are each compared in the passive component 11 and in the active component 10. In principle, data packets are not read into the input area 26 of the passive component 11 via the serial interface 22 until the input area 17 of the active component 11 is ready to receive these data packets. The status of the input area 26 is detected via the sequence counter 28, while the status of the input area 17 is detected by the acknowledgement counter 19. The two bytes i-2 and o-2 (cf. tables 1 and 2) each represents the current status or counter reading of the sequence counter 28 or acknowledgement counter 19. When new data packets arrive at the serial interface 22 of the passive component 11, the comparator device 29 of the control device 23 checks the identity of the bytes i-2 and o-2. Given identity, the incoming data packets are allowed to be entered in the input area 26. Given non-identity, the incoming data packets must be buffered in the buffer 30. It is to be noted that the buffer can also be part of the memory 24, in particular

if the latter is embodied as a RAM. When incoming data packets are stored in the input area 26, the received data is entered into the input area 26 starting from the byte i-7 (cf. table 2). The overall length of the received data packets is entered in the byte i-6 taking into account the length specification which is preset in the byte o-5. The byte i-2 is then incremented by +1 by the sequence counter 28, as a result of which the byte i-2 and o-2 are different.

The active component 10, i.e. comparator device 20 of the control device 14 detects the difference between the bytes o-2 and i-2 and reads the input data out of the input area 26 into the input area 17. Here, the error status can be obtained from the byte i-3. If the error status is not equal to 0, a serial error was detected when the data packets were received via the serial interface 22. The new data packets which have been read into the input area 17 of the active component 10 are then read out of the input area 17 for further use, for example into other passive components of the bus system in order to actuate them. The release of the input area 17 is shown by the active component 10 in which the acknowledgement counter 19 increments the byte o-2 by the value +1, so that the bytes o-2 and i-2 have the same value again. The identity between i-2 and o-2, which is detected by the comparator device 29 in the passive component 11, indicates to the latter that new data packets can be entered into the input area 26.

The byte o-3 (command byte) shown in table 1 has no significance if it has the value 0. However, if the value 1 is set, the input area 26 of the passive component 11 is cleared in each case before new data packets which are to be read out from the output area 16 of the active component 10 via the serial interface 22. In this case, the control device 23 of the passive component 11 sets the byte

i-2, i.e. the sequence counter 28, to the value of the byte o-2, i.e. the value of the sequence counter 18.

Furthermore, it is to be noted that it is not absolutely necessary to provide buffering of the data in the passive component 11 in the buffer 30 when data is read out via the serial interface 22. In this case, the buffering may, however, be useful because from the point of view of a passive component 11, the output area 25 is ready to receive again as quickly as possible so that new data packets can be transmitted from the output area 16 into the output area 25 of the passive component 11 by the active component 10. However, when data is read in via the serial interface 22 of the passive component 11, it is important to buffer the incoming data packets in the buffer 30 so that incoming data can be read in without delay. An overflow of the buffer 30 in this case is indicated in the output byte i-3 (cf. tables 2 and 3).

When the active component 10 fails, a watchdog which is prescribed by the corresponding standard, for example the PROFIBUS standard, must be detected by the passive component 11. Here, the last data packet of the active component 10 which was still completely received is read out of the output area 25 of the passive component 11 via the serial interface 22. When there is a network failure, no further data packets are received via the serial interface 22 of the passive component 11. Any data in the buffer 30 is rejected by the passive component. In the case of a network failure, or after such a failure, the entire input area of the passive component 11 is set to 0. As a result, a data packet which is received via the serial interface 22 and has the length 0 plus error status in the byte i-3 = 0, which corresponds to a synchronization message, is implicitly transmitted. If the passive component 11 can no longer be addressed via

the bus system, owing, for example, to a network fault, the entire output area 16 of the active component 10 is set to 0. As a result, one or more data packets with the length 0 are implicitly transmitted to the passive component, i.e. a synchronous message.

When the passive component 11 is activated by the bus system and when it is integrated into the bus system, synchronization is necessary. Here, all the output data is set to zero by the active component 10 in the output area 16 with the exception of the byte o-3. The byte o-3 is set to 1 and thus indicates that the passive component 11 should reset its input area, i.e. to 0.

This means that all the data in the input area 26 of the passive component 11 is cleared.

Claims

1. A passive component (11) for a bus system comprising having a bus interface (21) for connection to a bus, a serial interface (22) for serially reading out and reading in data, a data memory (24) with an output area (25) for storing data that has been read in via the bus interface (21) and is to be read out via the serial interface (22), and an input area (26) for storing data which has been read in via the serial interface and is to be read out via the bus interface, and a control device (23) for controlling the transmission and storage of data, detection means (27, 28) for detecting the status of the output area and of the input area and providing corresponding status information being provided, which status information is used as the basis for reading data into the output area and reading data out of the input area via the bus interface when the bus system is connected.

2. The passive component (11) as claimed in claim 1, characterized in that comparative means (29) are provided for periodically comparing the status information with corresponding status information of an active component of a connected bus system, the control device (23) controlling the reading in and reading out of data on the basis of this periodic comparison.

3. The passive component (11) as claimed in claim 2, characterized in that a data packet is not read out of a corresponding output area of the active component and into the output area (25) until the latter is ready to receive this data packet.

4. The passive component (11) as claimed in claim 3, characterized in that a buffer (30) for buffering a data packet which is to be read out of the output area via the serial interface (22) is provided.

5. The passive component (11) as claimed in claim 3 or 4, characterized in that the data packet is not read into the input area (26) via the serial interface until a corresponding input area of the active component is ready to receive this data packet.

6. The passive component (11) as claimed in claim 5, characterized in that a buffer (30) is provided which buffers a data packet, to be read into the input area via the serial interface (22), if the input area of the active component is not yet ready to receive it.

7. The passive component (11) as claimed in one of claims 1 to 6, characterized in that the detection means comprise an acknowledgement counter (27) for counting data packets which are read out via the serial interface (22), and a sequence counter (28) for counting data packets which are read in via the serial interface (22), the counting values serving as the status information.

8. The passive component (11) as claimed in one of claims 1 to 7, characterized in that the maximum size of the input area (26) and that of the output area (25) can be set in a variable fashion, the

data packets which are to be stored therein being able to have any desired sizes within the respectively set maximum size.

9. An active component (10) for exchanging data with a passive component (11) as claimed in one of the preceding claims, having a bus interface (13) for connection to a bus, a data memory (15) with an output area (16) for storing data which is to be stored in the output area (15) of the passive component (11) and is to be read out via its serial interface (22), and an input area (17) of data which is read out of the input area (26) of the passive component (11), and a control device (14) for controlling the transmission and the storage of data, detection means (18, 19) for detecting the status of the output area (16) and of the input area (17) and providing corresponding status information being provided, which status information is used by the active component (10) as the basis for reading data from the passive element (11) into the input area (17) via the bus interface (13) and reading data out of the output area (18) to the passive component (11).

10. The active component (10) as claimed in claim 9, characterized in that comparative means (20) are provided for periodically comparing the status information with corresponding status information of the passive component (11), the control device (14) controlling the reading in and reading out of the data on the basis of this periodic comparison.

11. The active component (10) as claimed in claim 9 or 10, characterized

in that a serial interface (12) for serially reading data into the output area (16) and for serially reading data out of the input area (17) is provided.

12. The active component (10) as claimed in claim 11, characterized in that a data packet is not read into the output area (16) of the active component via the serial interface (12) until the output area (25) of the passive component (11) is ready to receive this data packet.

13. The active component (10) as claimed in claim 11 or 12, characterized in that a data packet which is to be read out via the serial interface (12) is not read from the input area (26) of the passive component (11) into the input area (17) of the active component (10) until the input area (17) of the active component is ready to receive this data packet.

14. The active component (10) as claimed in on of claims 9 to 13, characterized in that the detection means comprise an acknowledgement counter (19) for counting data packets which are read out via the serial interface (12), and a sequence counter (18) for counting data packets which are read in via the serial interface (12), the counting values serving as the status information.

15. The active component (10) as claimed in one of claims 9 to 14, characterized in that the maximum size of the input area (17) and that of the output area (16) can be set in a variable fashion, the data packets which are to be stored therein being able to have any desired size within

the respectively set maximum size.

16. A method for reading serial data into and out of a bus system which comprises a passive component (11) with a serial interface (22) and a data memory (24) which has an output area (25) for reading out data via the serial interface (22) and an input area (26), and comprises an active component (10) with a data memory (15) which has an output area (16) and an input area (17), the statuses of the output areas (16, 25) and of the input areas (17, 26) being detected and corresponding status information being provided, which is used as the basis for the reconciliation of the output area (26) of the active component (10) and the output area (25) of the passive component (11), and of the input area (26) of the passive component (11) and the input area (17) of the active component (10).

17. The method as claimed in claim 16, characterized in that the status information of the output areas (16, 25) of the active and passive components are compared and the status information of the input areas (17, 26) of the active and passive components are periodically compared, the reconciliation of the output areas and of the input areas being carried out on the basis of this comparison.

18. The method as claimed in claim 16 or 17, characterized in that a data packet is not read into the output area (16) of the active component (10) until the output area (25) of the passive component (11) is ready to receive this data packet.

19. The method as claimed in claim 16, 17 or 18, characterized in that a data packet is not read from the input area (26) of the passive component (11) into the input area (17) of the active component (10) until the input area of the active component is ready to receive this data packet.

20. The method as claimed in one of claims 16 to 19, characterized in that the read-out data packets and the read-in data packets are counted, the counting values serving as the status information.

21. The method as claimed in one of claims 16 to 20, characterized in that the maximum size of the input areas (17, 26) and that of the output areas (16, 25) can be set in a variable fashion, the data packets which are to be stored therein being able to have any desired size within the respectively set maximum size.

Abstract

Serial data transmission via a bus system

The present invention relates to a passive component (11) for a bus system, such as, for example, a field bus system, having a bus interface (21) for connection to a bus, a serial interface (22) for serially reading out and reading in data, a data memory (24) with an output area (25) for storing data which has been read in via the bus interface (21) and is to be read out via the serial interface (22) and an input area (26) for storing data which has been read in via the serial interface and is to be read out via the bus interface, and a control device (23) for controlling the transmission and storage of data, detection means (27, 28) for detecting the status of the output area and of the input area and providing corresponding status information being provided, which status information is used as the basis for reading data into the output area and reading data out of the input area via the bus interface when the bus system is connected. The present invention also comprises a corresponding active component (10) for exchanging data with such passive component (11), and a method for reading data in and out of a bus system which comprises such a passive component (11) and such an active component (10).

The present invention makes data communication possible between such a bus system and one or more decentralized peripherals or serial interfaces.

(Fig. 3)

Claims

1. A passive component (11) for a bus system comprising having a bus interface (21) for connection to a bus, a serial interface (22) for serially reading out and reading in data, a data memory (24) with an output area (25) for storing data that has been read in via the bus interface (21) and is to be read out via the serial interface (22), and an input area (26) for storing data which has been read in via the serial interface and is to be read out via the bus interface, and a control device (23) for controlling the transmission and storage of data, detection means (27, 28) for detecting the status of the output area and of the input area and providing corresponding status information being provided, which status information is used as the basis for reading data into the output area and reading data out of the input area via the bus interface when the bus system is connected.

2. The passive component (11) as claimed in claim 1, characterized in that comparative means (29) are provided for periodically comparing the status information with corresponding status information of an active component of a connected bus system, the control device (23) controlling the reading in and reading out of data on the basis of this periodic comparison.

3. The passive component (11) as claimed in claim 2, characterized in that a data packet is not read out of a corresponding output area of the active component and into the output area (25) until the latter is ready to receive this data packet.

4. The passive component (11) as claimed in claim 3, characterized in that a buffer (30) for buffering a data packet which is to be read out of the output area via the serial interface (22) is provided.

5. The passive component (11) as claimed in claim 3 or 4, characterized in that the data packet is not read into the input area (26) via the serial interface until a corresponding input area of the active component is ready to receive this data packet.

6. The passive component (11) as claimed in claim 5, characterized in that a buffer (30) is provided which buffers a data packet, to be read into the input area via the serial interface (22), if the input area of the active component is not yet ready to receive it.

7. The passive component (11) as claimed in one of claims 1 to 6, characterized in that the detection means comprise an acknowledgement counter (27) for counting data packets which are read out via the serial interface (22), and a sequence counter (28) for counting data packets which are read in via the serial interface (22), the counting values serving as the status information.

8. The passive component (11) as claimed in one of claims 1 to 7, characterized in that the maximum size of the input area (26) and that of the output area (25) can be set in a variable fashion, the

data packets which are to be stored therein being able to have any desired sizes within the respectively set maximum size.

9. An active component (10) for exchanging data with a passive component (11) as claimed in one of the preceding claims, having a bus interface (13) for connection to a bus, a data memory (15) with an output area (16) for storing data which is to be stored in the output area (15) of the passive component (11) and is to be read out via its serial interface (22), and an input area (17) of data which is read out of the input area (26) of the passive component (11), and a control device (14) for controlling the transmission and the storage of data, detection means (18, 19) for detecting the status of the output area (16) and of the input area (17) and providing status information corresponding to the statuses, which status information is used by the active component (10) as the basis for reading data from the passive element (11) into the input area (17) via the bus interface (13) and reading data out of the output area (18) to the passive component (11).

10. The active component (10) as claimed in claim 9, characterized in that comparative means (20) are provided for periodically comparing the status information with corresponding status information of the passive component (11), the control device (14) controlling the reading in and reading out of the data on the basis of this periodic comparison.

11. The active component (10) as claimed in claim 9 or 10, characterized

in that a serial interface (12) for serially reading data into the output area (16) and for serially reading data out of the input area (17) is provided.

12. The active component (10) as claimed in claim 11, characterized in that a data packet is not read into the output area (16) of the active component via the serial interface (12) until the output area (25) of the passive component (11) is ready to receive this data packet.

13. The active component (10) as claimed in claim 11 or 12, characterized in that a data packet which is to be read out via the serial interface (12) is not read from the input area (26) of the passive component (11) into the input area (17) of the active component (10) until the input area (17) of the active component is ready to receive this data packet.

14. The active component (10) as claimed in on of claims 9 to 13, characterized in that the detection means comprise an acknowledgement counter (19) for counting data packets which are read out via the serial interface (12), and a sequence counter (18) for counting data packets which are read in via the serial interface (12), the counting values serving as the status information.

15. The active component (10) as claimed in one of claims 9 to 14, characterized in that the maximum size of the input area (17) and that of the output area (16) can be set in a variable fashion, the data packets which are to be stored therein being able to have any desired size within

the respectively set maximum size.

16. A method for reading serial data into and out of a bus system which comprises a passive component (11), forming a slave station, with a serial interface (22) and a data memory (24) which has an output area (25) for reading out data via the serial interface (22) and comprises an input area (26), and an active component (10), forming a master station, with a data memory (15) which has an output area (16) and an input area (17),

- a passive component (11) transfering data only at the request of an active component (10),
- the statuses of the output areas (16, 25) and of the input areas (17, 26) being detected and status information corresponding to the statuses being provided, which status information is used as the basis for the transfer of the data of the output area (16) of the active component (10) into the output area (25) of the passive component (11), and the transfer of the data of the input area (26) of the passive component (11) into the input area (17) of the active component (10).

17. The method as claimed in claim 16, characterized in that the status information of the output areas (16, 25) of the active and passive components are compared and the status information of the input areas (17, 26) of the active and passive components are periodically compared, the reconciliation of the output areas and of the input areas being carried out on the basis of this comparison.

18. The method as claimed in claim 16 or 17, characterized in that a data packet is not read into the output area (16) of the active component (10) until the output area (25) of the passive component (11) is ready to receive this data packet.

19. The method as claimed in claim 16, 17 or 18, characterized in that a data packet is not read from the input area (26) of the passive component (11) into the input area (17) of the active component (10) until the input area of the active component is ready to receive this data packet.

20. The method as claimed in one of claims 16 to 19, characterized in that the read-out data packets and the read-in data packets are counted, the counting values serving as the status information.

21. The method as claimed in one of claims 16 to 20, characterized in that the maximum size of the input areas (17, 26) and that of the output areas (16, 25) can be set in a variable fashion, the data packets which are to be stored therein being able to have any desired size within the respectively set maximum size.

Sub Spec (marked version)

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~~Description~~

SERIAL DATA TRANSMISSION VIA A BUS SYSTEM

CLAIM FOR PRIORITY

This application claims priority to International Application No. PCT/DE00/03109 which was published in the German language on September 7, 2000.

TECHNICAL FIELD OF THE INVENTION

The present invention relates to the transmission of serial data via a bus system, and in particular, to the transmission of serial data via a V.24 interface via a field bus.~~, for example the PROFIBUS DP. In particular, the present invention relates to a passive component and an active component for the bus system, at least the passive component having a serial interface for the reading in and reading out of data. Furthermore, the present invention relates to a method for the reading in and reading out of serial data via a bus system.~~

BACKGROUND OF THE INVENTION

Bus systems are in use in a wide variety of technical applications. In particular field buses, for example the PROFIBUS (PROcesFieldBUS) according to DIN 19245 (EN 50170 since 1996) are widely used, for example, in automation technology, for the transmission of data over relatively long paths. In contrast to most systems which transmit data in a parallel fashion, the PROFIBUS is a serial bus system in which data is transmitted serially. Field buses have wide-ranging fields of application because they can be connected to, and operated with, both simple and complex components (stations). Furthermore, they are advantageous in terms of the low connection costs and reduced expenditure on cabling. Additional advantages are short reaction times and simple protocols which make field ~~busses~~ buses real-time-capable. Other factors to note are the high degree of immunity to faults, even over large distances, simple integration in the ~~existance~~

existence of the systems and the ease with which the respective elements are made independently irreplaceable.

An example of such a field bus is the PROFIBUS according to DIN 19245, which can be divided into various hierarchical layers on the basis of different functionalities and modes of operation. Part 1 of DIN 19245 in this case defines the PROFIBUS layers 1 and 2, where the fieldbus datalink (FDL) is defined, for example. An example of the bus system of these layers is illustrated in Fig. 1. Part 2 of DIN 19245 defines the PROFIBUS layer 7 and contains the fieldbus message specification (FMS). Part 3 of DIN 19245 defines the PROFIBUS DP (decentralized peripherals) which comprises the PROFIBUS FDL of layers 1 and 2 and defines service interfaces and data interfaces for exchanging data with external peripheral data.

A fieldbus such as the PROFIBUS DP usually comprises one or more active stations and a plurality of passive stations. The active and passive stations or components are configured here in a master-slave relationship. This means that the active components actuate the passive components and/or read data in and out. The passive components operate only after being actuated by the active components. The problem with such ~~fieldbusses~~ fieldbuses is the reading out of the current data to external peripherals, such as for example computers. Existing systems are slow, inefficient and complicated.

SUMMARY OF THE INVENTION

The present invention relates to the transmission of serial data via a bus system, and in particular, to the transmission of serial data via a V.24 interface via a field bus, such as the PROFIBUS DP. In particular, the present invention relates to a passive component and an active component for the bus system, at least the passive component having a serial interface for the

reading in and reading out of data. Furthermore, the present invention relates to a method for the reading in and reading out of serial data via a bus system.

~~The object of the present invention is thus to provide~~ In one embodiment of the invention, there is a passive component for a bus system, an active component for a bus system and a method for reading data in and out of a bus system which permit rapid, efficient and reliable reading out and reading in of data to or from one or more of the central peripherals.

~~This object is achieved by means of a passive component for a bus system as claimed in claim 1, comprising having~~ The system includes, for example, a bus interface for connection to a bus, a serial interface for serially reading out and reading in data, a data memory with an output area to the memory of data which has been read in via the bus interface and is to be read out via the serial interface, and an input area for storing data which has been read in via the serial interface and is to be read out via the bus interface, and a control device for controlling the transmission and storage of data, a detection device to detect ~~means for detecting~~ the status of the output area and of the input area and providing corresponding status information being provided, which status information is used as the basis for reading data in via the output area and reading data out of the input area via the bus interface when the bus systems are connected.

~~The object above is also achieved by means of~~ In one aspect of the invention, there is an active component for exchanging data with such a passive component ~~as claimed in claim 9,~~ having, for example, a bus interface for connection to a bus, a data memory with an output area for storing data which is to be stored in the output area of the passive component and is to be read out via its serial interface, and an input area of data which is read out of the input area of the

passive component, and a control device for controlling the transmission and storage of data, a detection device to detect ~~means for detecting~~ the status of the output area and of the input area and for providing corresponding status information being provided, which status information is used by the active component as the basis for reading data from the passive component into the input area via the bus interface and for transmitting data from the output area to the passive component.

~~The object above is also achieved by means of~~ In another embodiment of the invention, there is a method for reading serial data into and out of a bus system~~ as claimed in claim 16, the~~ The bus system includes, for example, ~~comprising~~ a passive component with a serial interface and a data memory which has an output area for reading out data via the serial interface and an input area, and comprises an active component with a data memory which has an output area and an input area, the statuses~~es~~ of the output areas and of the input areas being detected and corresponding status information being provided, which is used as the basis for the reconciliation of the output area of the active component and the output area of the passive component, and of the input area of the passive component and the input area of the active component.

The passive component according to the present invention advantageously has a comparative device to ~~means for~~ periodically ~~comparing~~ compare the status information with corresponding status information of the active component, the control device controlling the reading in and reading out of data on the basis of this periodical comparison. For example, in the ~~abovementioned~~ above-mentioned PROFIBUS DP system, in which the output areas and input areas of the active and passive components are reconciled cyclically, the input areas and output areas of the passive component according to the present invention, and the input areas

and output areas of the active component according to the present invention are reconciled, that is to say the data are copied, ~~only~~ if the status information indicates that the respective area has the corresponding predefined status which permits or requires the reconciliation of the data. For example, a data packet is not read out of the output area of the active component and into the output area of the passive component until the output area of the passive component is ready to receive this data packet. This means that first the respective data packet has to be read out of the output area of the passive component via the serial interface to a decentralized peripheral before a new data packet can be received. In this context, a buffer for buffering a data packet which is to be read out of the output area via the serial interface can be provided in the passive component in order to enable the output area of the passive component to be made vacant as quickly as possible so that a new data packet from the active component can be read in.

A data packet is furthermore advantageously not read into the input area of the passive component via the serial interface until the corresponding input area of the active component is ready to receive this data packet. In this case, ~~too,~~ it is possible to provide a buffer which buffers a data packet, to be read into the input area via the serial interface, if the input area of the active component is not yet ready to receive it.

The detection ~~means for detecting~~ <u>device to detect</u> the status of the output area and of the input area of the passive component advantageously comprise an acknowledgement counter for counting data packets which are read out via the serial interface of the passive component, and a sequence counter for counting data packets which are read in via the serial interface of the passive component, the counting values serving as the status information.

Furthermore, in the passive component according to the present invention, the maximum size of the input area and that of the output area can be set in a variable fashion, the data packets which are to be stored therein being able to have any desired size within the respectively set maximum size. As a result, a very flexible transmission of serial data in the bus system becomes possible.

The passive component described above and in accordance with the present invention is exclusively configured for the reading in and reading out of serial data via a corresponding serial interface, for example a V.24 interface. The active component according to the present invention in this case controls this reading in and reading out of data via the serial interface of the passive component. The data memory of the active component has an output area which is reconciled with the output area of the passive component according to the present invention, and also has an input area which is reconciled with the input area of the passive component according to the present invention. The active component according to the present invention can also have its own serial interface, for example a V.24 interface, for the serial reading of data into the corresponding output area for the serial reading of data out of the corresponding input area. Here, the data packet cannot be read into the output area of the active component via the serial interface until the output area of the passive component is ready to receive this data packet. On the other hand, a data packet which is to be read out via the serial interface of the active component cannot be read from the input area of the passive component into the input area of the active component until the input area of the active component is ready to receive this data packet. Similarly to the passive component, with the active component according to the present invention it is also advantageous if the detection ~~means for detecting~~

device to detect the status of the output area and of the input area comprise an acknowledgement counter for counting data packets read out via the serial interface, and a sequence counter for counting data packets read in via the serial interface, the target values serving as the status information. In the active element too, the maximum size of the input area and that of the output area can be set in a variable fashion, the data packets to be stored therein being able to have any desired size within the respectively set maximum size. The respective input area and the respective output area can have different sizes here. The size of the input areas and of the output areas are also predefined here for the passive component by the active component.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is explained in more detail below by ~~means of a preferred~~ exemplary ~~embodiment~~ embodiments and with reference to the appended drawings, in which

Fig. 1 shows a schematic view of a bus system ~~on which~~ in the present invention ~~can be applied,~~.

Fig. 2 shows a schematic view of a bus system with higher-value services than the bus system shown in Fig. 1 which forms the basis for the present invention~~, and~~.

Fig. 3 shows a schematic view of an active component and of a passive component according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The PROFIBUS FDL system (shown in Fig. 1) of the layers 1 and 2 comprises a line-like bus structure in which active components (stations) 1a, 1b and 1c with the addresses 1, 8 and 25 are connected to a bus 4 via spur lines. The bus 4 has a line shape and is terminated at

both ends by a bus termination 4. Passive components (stations) 2a, 2b, 2c and 2d with the addresses 3, 4, 9 and 39 are also connected to the bus 4 by spur lines. The address data items are of course examples.

The overall length of the bus 4 can be up to 1.2 km, while the spur lines to the active and passive components are 0.3 m long at maximum. The overall number of subscribers, i.e. the overall number of active and passive components is restricted to a maximum of 126. The active components 1a, 1b and 1c are connected by a logic token ring, that is to say a decentralized bus access takes place in accordance with the token passing principle. A central bus access is subordinated to this superordinate decentralized passive access in accordance with the master-slave principle. The active components 1a, 1b and 1c are the master stations and form the logic token ring. Each component which has the token can carry out corresponding useful data services. The passive components 2a, 2b, 2c and 2d are slave stations which react to the access by the active components. The active components change data with one another, and the respective active station which is in possession of the token can actuate the other active and passive components. The passive components transmit and receive data only at the request of the active stations and do not participate in the active bus operation.

Each active component and each passive component has an electrical bus interface via which data is exchanged with other components. In the case of the PROFIBUS FDL as well as in the case of the PROFIBUS DP, for example RS 485 interfaces are used which permit data communication with a plurality of other components on the basis of 11 bit/characters (startbit/stop-bit/paritybis, 8 useful data bits).

Figure 2 shows an example of a PROFIBUS DP Monomaster system with an active component 1 (DP Master/Class 1)

and a plurality of passive components 2a, 2b, 2c and 2d (DP slaves A, B, C and D) according to the present invention. The PROFIBUS DP comprises services of the PROFIBUS FDL which are described with respect to the in Fig. 1 and also defines higher-value services, namely service interfaces or data interfaces for communicating with their decentralized peripherals, as shown in Fig. 2. These functionalities of the active component 1 in the PROFIBUS DP system comprise here the data transfer via a data interface 5, via input data areas (input data) 6 and output data areas (output data) 7, and also configuration, stages detection and diagnostics. The passive stations 2a, 2b, 2c and 2d each have an input area (input) and an output area (output). The passive component 2a comprises here an input area 8a and an output area 9a, the passive component 2b comprises an input area 8b and an output area 9b, the passive component 2c comprises an input area 8c and an output area 9c and the passive component 2d comprises an input area 8d and an output area 9d. ~~All the~~ The passive components 2a, 2b, 2c and 2d are connected to the linear bus 4 via short spur lines, as is the active component 1. A large data memory is provided in the active component 1 and in it ~~in each case~~ the input areas and output areas of the passive components are mirrored, that is to say are present in identical forms. For this purpose, the active component 1 updates its input areas 6 and output areas 7 cyclically with those of the passive components. The output areas 9a, 9b, 9c and 9d of the passive components contain here the data which is to be read out from the passive components to respectively decentralized peripherals, and the input areas 8a, 8b, 8c and 8d contain the data which is to be read from respective decentralized peripherals into the passive components. The input area 6 of the active component 1 contains data to be read out from the active component 1 to a decentralized peripheral, while the output area 7 of the active component 1 contains data which is to be read in from such a decentralized peripheral.

Fig. 3 is a schematic illustration of an active component 10 according to the present invention and of a passive component 11 according to the present invention. The active component 10 and the passive component 11 as illustrated in Fig. 3 can be integrated, for example, as an active component 1 or passive component 2a, 2b, 2c or 2d into the bus systems shown in Figs. 1 and 2.

The passive component 11 which is shown in Fig. 3 comprises a bus interface 21 for connecting the passive component 11 to a bus, such as for example a field bus, as has been described above. Furthermore, the passive component comprises a serial interface 22, for example a V.24 interface for serially reading in and reading out data into and out of a peripheral, such as for example a computer. Furthermore, a data memory 24 with an output area 25 for storing data which has been read out via the bus interface 21 and is to be read in via the serial interface 22, and an input area 26 for storing data which has been read in via the serial interface 22 and is to be read out via the bus interface 21 is provided. The transmission and storage of data is controlled by a control device 23, an acknowledgement counter 27 for counting data packets which are read out via the serial interface 22, and a sequence counter 28 for counting data packets which are read in via the serial interface 22 being provided. The respective counting values serve as the status information with respect to the data packets stored in the output area 25 and input area 26. The acknowledgement counter 27 is embodied as part of the output area 25, while the sequence counter 28 is embodied as part of the input area 26. The data memory 24, which comprises the output area 25 and the input area 26, is, for example, a RAM (Random Access Memory). The control device 23 of the passive component 11 comprises a comparative device ~~means~~ 29 ~~for~~ to periodically ~~comparing~~ compare the status information

with corresponding status information of the active element 10, the control device 23 controlling the reading in and reading out of data via the output area 25 and the input area 26 on the basis of this periodic comparison. An optional buffer 30 for buffering data packets which are to be read out of the output area via the serial interface 22 is provided between the control device 23 and the serial interface 22. The buffer 30 is also used for buffering a data packet which is to be read into the input area 26 via the serial interface 22. The maximum size of the input area 26 and of the output area 25 of the passive component 11 can be set in a variable fashion, the data packets which are to be stored therein being able to have any desired size within the respectively set maximum size, as is explained in detail below.

The passive component 11 which is illustrated in Fig. 3 is connected to a correspondingly assigned active element 10 via its bus interface 21 with a bus system, for example a field bus such as the PROFIBUS DP. The active element 10 correspondingly comprises a bus interface 13 with which it is connected to the bus system. In addition, the active component comprises a data memory 15, for example a RAM, with an output area 16 for storing data which is to be stored in the output area 25 of the passive element 11 and data which is to be read out via its serial interface 22, and an input area 17 of data which has been read out of the input area 26 of the passive component 11. As has been explained above, the data of the output area 16 of the active component 10 and of the output area 25 of the passive component 11 is cyclically mirrored and/or reconciled, like the data of the input area 17 of the active component 10 and the data of the input area 26 of the passive component 11. Here, the data of the output area 16 of the active component 10 is transferred in the output area 25 of the passive component 11, and the data of the input area 26 of the passive component 11 is transferred into the input area

17 of the active component 10. The active component 10 also comprises an optional serial interface 12 for serially reading data into the output area 16 and for serially reading data out of the input area 17. In addition, an acknowledgement counter 19 for counting data packets which have been read out via the serial interface 12, and a sequence counter 19 for counting data packets which have been read out via the serial interface 12 and a sequence counter 18 for counting data packets which have been read in via the serial interface 12 are provided, the counting values serving as the status information, which is used as the basis for the reading of data from the passive component 11 into the input area 17 via the bus interface 13 and for the reading of data out of the output area 18 to the passive component 11. The transmission of data is controlled here by the control device 14 which comprises a comparative ~~means~~ device 20 ~~for~~ to periodically ~~comparing~~ compare the status information with corresponding status information of the passive component 11, the control device 14 controlling the reading in and reading out of data on the basis of this periodical comparison. The acknowledgement counter 19 is embodied as part of the input area 17, and the sequence counter 18 is embodied as part of the output area 16.

Like the input area 26 and the output area 25 of the passive component 11, the input area 17 and the output area 16 of the active component 10 can also be set with respect to the maximum size, the data packets which are to be stored in them being able to have any desired size within the respectively set maximum size. The maximum size of the input areas 17 and 26 and of the output areas 16 and 25 is set by the active component 10 when the bus system is initialized. For this purpose, the active component 10 sets up the data communication to the passive component 11 in accordance with EN 50 170 and DIN 19 245 when operation is started and transmits a diagnostic message to the passive

component 11. The passive component 11, i.e. the control device 23 receives the diagnostic message and signals the corresponding diagnostic parameters back to the active component 10, i.e. its control device 14. The control device 14 of the active component 10 then transmits the parameters to be set to the control device 23 of the passive component 11, as a result of which the latter is parameterized and configured. The setting of the parameters is correspondingly acknowledged by the passive element 11, in response to which the active component 10 transmits a configuration message to the passive component 11. From the configuration message, the passive component 11 detects the data area size for the input area 26 and the output area 25 and sets their sizes correspondingly. The sizes can be defined here in, for example, the limits 7 bytes to 244 bytes. The data area sizes which are set are then acknowledged by the passive component 11. During the further course of the operation, the data is cyclically updated in the input areas 17 and 26 and the output areas 16 and 25. The abovementioned variable setting of the sizes of the output areas and of the input areas is supported in a corresponding way by corresponding algorithms in the control devices 14 and 23.

~~It is to be emphasized that the~~ The passive component 11 according to the present invention is used exclusively for data communication between the bus system and one or more peripherals by means of the serial interface 22 and does not have require any further functions. However, it is also conceivable for the active component 11 according to the present invention to perform additional control or sensor functions in the bus system. ~~In all cases the~~ The data which is to be read out of the output area 16 of the active component 10 to the output area 25 of the passive component 11 and then via the serial interface 22 of the passive component 11 generally ~~constitutes~~ includes data which is used to actuate passive components of the bus system which perform control,

sensor and actuator functions and the like. The data which has been read via the serial interface 22 of the passive component into the input area 26 and from there into the input area 17 of the active component 11 ~~constitutes~~ includes data which comprises the messages of the corresponding peripheral, connected to the serial interface 22, to the active component 10, these messages being able to be used in turn for actuating other passive components of the bus system, for example.

In the passive component 11 according to the present invention, the data which is used within the bus system is thus converted into output data which is read out via the serial interface 22 to one or more decentralized peripherals, the serial interface 22 being able to be, for example, a V.24 or a RS 232 interface. On the other hand, the passive component 11 according to the present invention of one or more decentralized peripherals into the bus system converts data from serial data into data which has the data format necessary for the bus system.

In order to be able to transmit data between the bus system and one or more decentralized peripherals via the serial interface 22 of the passive component 11 or via the serial interface 12 of the active component 10, according to the present invention a further communications protocol, which is defined for example as in the following tables 1 and 2 is superimposed on the input areas 17 and 25 and the output areas 16 and 24. The serial interfaces 12 and 22 are given in this example as V.24 interfaces.

Table 1 presents the communications protocol for the output areas 16 and 24, that is to say the data transmission device from the active component to the passive component 11 for reading out the data via the serial interface 22 (V.24 interface) of the passive component 11.

Byte No.	Designation	Function
o-1	tx_seq	Sequence counter transmission of a V.24 telegram
o-2	rx_seq_ack	Acknowledgement counter for reception of a V.24 telegram
o-3	Command	Bit 0 0 no significance 1 reset of reception buffer DP slave before the new telegram is transmitted Bits 1..7 reserved
o-40	Reserved	00
o-5	rx_pref_len	Preset maximum byte number of a received telegram, if the value 00 is entered here the reception length is independently determined by the DP slave.
o-6	tx_len	Length data [byte] of telegram to be transmitted
o-7	Data 1	First octet to be transmitted via V.24
o-8	Data 2	Second octet to be transmitted via V.24
	Data...	...
o-(txlen + 6)	Data [tx_len]	Last octet to be transmitted via V.24

Table 2 represents the communications protocol for the input areas 17 and 26, i.e. the data transmission device from the passive component 11 to the active component 10 for data packets (telegrams) which have been received via the serial interface 22 (V.24 interface) of the passive component 11.

Byte No.	Designation	Function
i-1	tx_seq_ack	Acknowledgement counter for transmit data V.24
i-2	rx_seq	Sequence counter for reception of a V.24 telegram
i-3	rx_tx_fail	Fault message DP-slave, for format see below.
i-4	Reserved	00

i-5	Reserved	00
i-6	rx_len	Length data [byte] of the received telegram, the maximum length given in the range o-5 is not exceeded (provided <>0).
i-7	Data 1	Received data 1
i-8	Data 2	Received data 2
:	:	:
i-rx len+6	Data [rx_len]	Last octet received data

The reception buffer of the passive component 11 is the buffer 30 for buffering data packets which are to be read in or read out.

The following table 3 represents an example of the display of fault messages of the passive component 11 in the component i-3 of the communications protocol for the input areas.

Bit position	Significance
0	Reception buffer overflow
1	Reception error, frame error
2	parity error
3	Other reception errors
4	Reserved (=0)
5	Reserved (=0)
6	Reserved (=0)
7	Internal PROFIBUS DP-slave error

If there is error-free transmission, i.e. error-free reading in of data via the serial interface 22 into the reception memory or buffer (reception buffer) 30 into the input area 26, the byte i-3 is equal to 0. In the case of an error, i.e. if i-3 is unequal to 0, the received data are nevertheless to be read into the input area 26 via the buffer 30 and thus read into the input area 17 of the active component 11 by means of the cyclical reading out via the bus system.

The principle of the transmission mechanism for transmitting data packets data packets to be out of the output area 16 and into the output area 25 and via the serial interface 22 to one or more peripherals will be explained below. The transmission mechanism is based here on a comparison of the bytes o-1 and i-1 of the transmission protocols such as are illustrated, for example, in tables 1 and 2, in the comparator device 20 of the control device 14 of the active component 10 and the comparative device 29 of the control device 23 of the passive component 11. This means that the status or the current counter reading of the sequence counter 18 of the output area 16 and of the acknowledgement counter 27 of the output area 25 are compared. The two counter readings are each contained in byte o-1 and i-1. In principle, a data packet is not read out of the output area 16 of the active component 10 and into the output area 25 of the passive component 11 until the output area 25 is ready to receive this data packet, i.e. the output area 25 is empty. In order to speed up the reading of data packets out of the output area 16 of the active component 10 and into the output area 25 of the passive component 11, the data which is to be read out of the output area 25 via the serial interface 22 is buffered in the buffer 30.

When the data is read out, the control device 14 of the active component 10 firstly checks the bytes o-1 and i-1 for identity. Given identity, data packets which are to be read out can be entered into the output memory 16 of the active component 10 and the data is then, in cyclical reading out, copied into the output area 25 of the passive component 11, from which it is then read out via the serial interface 22. Given non-identity between the bytes o-1 and i-1, the transmission mechanism is still occupied, i.e. the reading of data out of the output area 25 via the serial interface 22 is not yet terminated so that no new data packets are allowed to be entered into the output area 16 of the active component 10. Given identity between the two bytes, data packets which are

to be read out are thus entered into the output area 16 of the active component 10 starting from the byte o-7. The overall length of the data is entered in the byte o-6. The byte o-1 is then incremented by the value +1, as a result of which the bytes o-1 and i-1 are differentiated. As long as this difference exists, no new data is allowed to be entered into the output area 16 of the active component 10.

The passive component 11, i.e. the comparator device 29 of the control device 23 also compares the bytes o-1 and i-1 and, when a difference is detected between these two bytes, it transmits output data from the output area 25 to the serial interface 22 via the buffer 30. When the reading-out operation from the output area 25 is terminated, the byte i-1 is incremented by the value +1, so that the byes i-1 and o-1 again have the same value, with the result that new data packets can be read into the output area 16 of the active component 10.

The reception mechanism for receiving data via the serial interface 22 of the passive component 11 is equivalent. Here, the bytes i-2 and o-2 are each compared in the passive component 11 and in the active component 10. In principle, data packets are not read into the input area 26 of the passive component 11 via the serial interface 22 until the input area 17 of the active component 11 is ready to receive these data packets. The status of the input area 26 is detected via the sequence counter 28, while the status of the input area 17 is detected by the acknowledgement counter 19. The two bytes i-2 and o-2 (cf. tables 1 and 2) each represents the current status or counter reading of the sequence counter 28 or acknowledgement counter 19. When new data packets arrive at the serial interface 22 of the passive component 11, the comparator device 29 of the control device 23 checks the identity of the bytes i-2 and o-2. Given identity, the incoming data packets are allowed to be entered in

the input area 26. Given non-identity, the incoming data packets must be buffered in the buffer 30. It is to be noted that the buffer can also be part of the memory 24, in particular if the latter is embodied as a RAM. When incoming data packets are stored in the input area 26, the received data is entered into the input area 26 starting from the byte i-7 (cf. table 2). The overall length of the received data packets is entered in the byte i-6 taking into account the length specification which is preset in the byte o-5. The byte i-2 is then incremented by +1 by the sequence counter 28, as a result of which the byte i-2 and o-2 are different.

The active component 10, i.e. comparator device 20 of the control device 14 detects the difference between the bytes o-2 and i-2 and reads the input data out of the input area 26 into the input area 17. Here, the error status can be obtained from the byte i-3. If the error status is not equal to 0, a serial error was detected when the data packets were received via the serial interface 22. The new data packets which have been read into the input area 17 of the active component 10 are then read out of the input area 17 for further use, for example into other passive components of the bus system in order to actuate them. The release of the input area 17 is shown by the active component 10 in which the acknowledgement counter 19 increments the byte o-2 by the value +1, so that the bytes o-2 and i-2 have the same value again. The identity between i-2 and o-2, which is detected by the comparator device 29 in the passive component 11, indicates to the latter that new data packets can be entered into the input area 26.

The byte o-3 (command byte) shown in table 1 has no significance if it has the value 0. However, if the value 1 is set, the input area 26 of the passive component 11 is cleared in each case before new data packets which are to be read out from the output area

16 of the active component 10 via the serial interface 22. In this case, the control device 23 of the passive component 11 sets the byte i-2, i.e. the sequence counter 28, to the value of the byte o-2, i.e. the value of the sequence counter 18.

Furthermore, it is to be noted that it is not absolutely necessary to provide buffering of the data in the passive component 11 in the buffer 30 when data is read out via the serial interface 22. In this case, the buffering may, however, be useful because from the point of view of a passive component 11, the output area 25 is ready to receive again as quickly as possible so that new data packets can be transmitted from the output area 16 into the output area 25 of the passive component 11 by the active component 10. However, when data is read in via the serial interface 22 of the passive component 11, it is important to buffer the incoming data packets in the buffer 30 so that incoming data can be read in without delay. An overflow of the buffer 30 in this case is indicated in the output byte i-3 (cf. tables 2 and 3).

When the active component 10 fails, a watchdog which is prescribed by the corresponding standard, for example the PROFIBUS standard, must be detected by the passive component 11. Here, the last data packet of the active component 10 which was still completely received is read out of the output area 25 of the passive component 11 via the serial interface 22. When there is a network failure, no further data packets are received via the serial interface 22 of the passive component 11. Any data in the buffer 30 is rejected by the passive component. In the case of a network failure, or after such a failure, the entire input area of the passive component 11 is set to 0. As a result, a data packet which is received via the serial interface 22 and has the length 0 plus error status in the byte i-3 = 0, which corresponds to a synchronization message, is implicitly transmitted. If the passive component 11 can

no longer be addressed via the bus system, owing, for example, to a network fault, the entire output area 16 of the active component 10 is set to 0. As a result, one or more data packets with the length 0 are implicitly transmitted to the passive component, i.e. a synchronous message.

When the passive component 11 is activated by the bus system and when it is integrated into the bus system, synchronization is necessary. Here, all the output data is set to zero by the active component 10 in the output area 16 with the exception of the byte o-3. The byte o-3 is set to 1 and thus indicates that the passive component 11 should reset its input area, i.e. to 0.

This means that ~~all~~ the data in the input area 26 of the passive component 11 is cleared.

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SERIAL DATA TRANSMISSION VIA A BUS SYSTEM

CLAIM FOR PRIORITY

This application claims priority to International Application No. PCT/DE00/03109 which was published in the German language on September 7, 2000.

TECHNICAL FIELD OF THE INVENTION

The present invention relates to the transmission of serial data via a bus system, and in particular, to the transmission of serial data via a V.24 interface via a field bus.

BACKGROUND OF THE INVENTION

Bus systems are in use in a wide variety of technical applications. In particular field buses, for example the PROFIBUS (PROcesFieldBUS) according to DIN 19245 (EN 50170 since 1996) are widely used, for example, in automation technology, for the transmission of data over relatively long paths. In contrast to most systems which transmit data in a parallel fashion, the PROFIBUS is a serial bus system in which data is transmitted serially. Field buses have wide-ranging fields of application because they can be connected to, and operated with, both simple and complex components (stations). Furthermore, they are advantageous in terms of the low connection costs and reduced expenditure on cabling. Additional advantages are short reaction times and simple protocols which make field buses real-time-capable. Other factors to note are the high degree of immunity to faults, even over large distances, simple integration in the existence of the systems and the ease with which the respective elements are made independently irreplaceable.

An example of such a field bus is the PROFIBUS according to DIN 19245, which can be divided into various hierarchical layers on the basis of different

functionalities and modes of operation. Part 1 of DIN 19245 in this case defines the PROFIBUS layers 1 and 2, where the fieldbus datalink (FDL) is defined, for example. An example of the bus system of these layers is illustrated in Fig. 1. Part 2 of DIN 19245 defines the PROFIBUS layer 7 and contains the fieldbus message specification (FMS). Part 3 of DIN 19245 defines the PROFIBUS DP (decentralized peripherals) which comprises the PROFIBUS FDL of layers 1 and 2 and defines service interfaces and data interfaces for exchanging data with external peripheral data.

A fieldbus such as the PROFIBUS DP usually comprises one or more active stations and a plurality of passive stations. The active and passive stations or components are configured here in a master-slave relationship. This means that the active components actuate the passive components and/or read data in and out. The passive components operate only after being actuated by the active components. The problem with such fieldbuses is the reading out of the current data to external peripherals, such as for example computers. Existing systems are slow, inefficient and complicated.

SUMMARY OF THE INVENTION

The present invention relates to the transmission of serial data via a bus system, and in particular, to the transmission of serial data via a V.24 interface via a field bus, such as the PROFIBUS DP. In particular, the present invention relates to a passive component and an active component for the bus system, at least the passive component having a serial interface for the reading in and reading out of data. Furthermore, the present invention relates to a method for the reading in and reading out of serial data via a bus system.

In one embodiment of the invention, there is a passive component for a bus system, an active component for a bus system and a method for reading data in and out of a bus system which permit rapid, efficient and reliable

reading out and reading in of data to or from one or more of the central peripherals.

The system includes, for example, a bus interface for connection to a bus, a serial interface for serially reading out and reading in data, a data memory with an output area to the memory of data which has been read in via the bus interface and is to be read out via the serial interface, and an input area for storing data which has been read in via the serial interface and is to be read out via the bus interface, and a control device for controlling the transmission and storage of data, a detection device to detect the status of the output area and of the input area and providing corresponding status information being provided, which status information is used as the basis for reading data in via the output area and reading data out of the input area via the bus interface when the bus systems are connected.

In one aspect of the invention, there is an active component for exchanging data with such a passive component having, for example, a bus interface for connection to a bus, a data memory with an output area for storing data which is to be stored in the output area of the passive component and is to be read out via its serial interface, and an input area of data which is read out of the input area of the passive component, and a control device for controlling the transmission and storage of data, a detection device to detect the status of the output area and of the input area and for providing corresponding status information being provided, which status information is used by the active component as the basis for reading data from the passive component into the input area via the bus interface and for transmitting data from the output area to the passive component.

In another embodiment of the invention, there is a method for reading serial data into and out of a bus

system. The bus system includes, for example, a passive component with a serial interface and a data memory which has an output area for reading out data via the serial interface and an input area, and comprises an active component with a data memory which has an output area and an input area, the statuses of the output areas and of the input areas being detected and corresponding status information being provided, which is used as the basis for the reconciliation of the output area of the active component and the output area of the passive component, and of the input area of the passive component and the input area of the active component.

The passive component according to the present invention advantageously has a comparative device to periodically compare the status information with corresponding status information of the active component, the control device controlling the reading in and reading out of data on the basis of this periodical comparison. For example, in the above-mentioned PROFIBUS DP system, in which the output areas and input areas of the active and passive components are reconciled cyclically, the input areas and output areas of the passive component according to the present invention, and the input areas and output areas of the active component according to the present invention are reconciled, that is to say the data are copied, if the status information indicates that the respective area has the corresponding predefined status which permits or requires the reconciliation of the data. For example, a data packet is not read out of the output area of the active component and into the output area of the passive component until the output area of the passive component is ready to receive this data packet. This means that first the respective data packet has to be read out of the output area of the passive component via the serial interface to a decentralized peripheral before a new data packet can be received. In this context, a buffer for buffering a data packet which is

to be read out of the output area via the serial interface can be provided in the passive component in order to enable the output area of the passive component to be made vacant as quickly as possible so that a new data packet from the active component can be read in.

A data packet is furthermore advantageously not read into the input area of the passive component via the serial interface until the corresponding input area of the active component is ready to receive this data packet. In this case, it is possible to provide a buffer which buffers a data packet, to be read into the input area via the serial interface, if the input area of the active component is not yet ready to receive it.

The detection device to detect the status of the output area and of the input area of the passive component advantageously comprise an acknowledgement counter for counting data packets which are read out via the serial interface of the passive component, and a sequence counter for counting data packets which are read in via the serial interface of the passive component, the counting values serving as the status information.

Furthermore, in the passive component according to the present invention, the maximum size of the input area and that of the output area can be set in a variable fashion, the data packets which are to be stored therein being able to have any desired size within the respectively set maximum size. As a result, a very flexible transmission of serial data in the bus system becomes possible.

The passive component described above and in accordance with the present invention is exclusively configured for the reading in and reading out of serial data via a corresponding serial interface, for example a V.24 interface. The active component according to the present invention in this case controls this reading in

and reading out of data via the serial interface of the passive component. The data memory of the active component has an output area which is reconciled with the output area of the passive component according to the present invention, and also has an input area which is reconciled with the input area of the passive component according to the present invention. The active component according to the present invention can also have its own serial interface, for example a V.24 interface, for the serial reading of data into the corresponding output area for the serial reading of data out of the corresponding input area. Here, the data packet cannot be read into the output area of the active component via the serial interface until the output area of the passive component is ready to receive this data packet. On the other hand, a data packet which is to be read out via the serial interface of the active component cannot be read from the input area of the passive component into the input area of the active component until the input area of the active component is ready to receive this data packet. Similarly to the passive component, with the active component according to the present invention it is also advantageous if the detection device to detect the status of the output area and of the input area comprise an acknowledgement counter for counting data packets read out via the serial interface, and a sequence counter for counting data packets read in via the serial interface, the target values serving as the status information. In the active element too, the maximum size of the input area and that of the output area can be set in a variable fashion, the data packets to be stored therein being able to have any desired size within the respectively set maximum size. The respective input area and the respective output area can have different sizes here. The size of the input areas and of the output areas are also predefined here for the passive component by the active component.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is explained in more detail below by exemplary embodiments and with reference to the appended drawings, in which

Fig. 1 shows a schematic view of a bus system in the present invention.

Fig. 2 shows a schematic view of a bus system with higher-value services than the bus system shown in Fig. 1 which forms the basis for the present invention.

Fig. 3 shows a schematic view of an active component and of a passive component according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The PROFIBUS FDL system (shown in Fig. 1) of the layers 1 and 2 comprises a line-like bus structure in which active components (stations) 1a, 1b and 1c with the addresses 1, 8 and 25 are connected to a bus 4 via spur lines. The bus 4 has a line shape and is terminated at both ends by a bus termination 4. Passive components (stations) 2a, 2b, 2c and 2d with the addresses 3, 4, 9 and 39 are also connected to the bus 4 by spur lines. The address data items are of course examples.

The overall length of the bus 4 can be up to 1.2 km, while the spur lines to the active and passive components are 0.3 m long at maximum. The overall number of subscribers, i.e. the overall number of active and passive components is restricted to a maximum of 126. The active components 1a, 1b and 1c are connected by a logic token ring, that is to say a decentralized bus access takes place in accordance with the token passing principle. A central bus access is subordinated to this superordinate decentralized passive access in accordance with the master-slave principle. The active components 1a, 1b and 1c are the master stations and form the logic token ring. Each

component which has the token can carry out corresponding useful data services. The passive components 2a, 2b, 2c and 2d are slave stations which react to the access by the active components. The active components change data with one another, and the respective active station which is in possession of the token can actuate the other active and passive components. The passive components transmit and receive data only at the request of the active stations and do not participate in the active bus operation.

Each active component and each passive component has an electrical bus interface via which data is exchanged with other components. In the case of the PROFIBUS FDL as well as in the case of the PROFIBUS DP, for example RS 485 interfaces are used which permit data communication with a plurality of other components on the basis of 11 bit/characters (startbit/stop-bit/paritybis, 8 useful data bits).

Figure 2 shows an example of a PROFIBUS DP Monomaster system with an active component 1 (DP Master/Class 1) and a plurality of passive components 2a, 2b, 2c and 2d (DP slaves A, B, C and D) according to the present invention. The PROFIBUS DP comprises services of the PROFIBUS FDL which are described with respect to the in Fig. 1 and also defines higher-value services, namely service interfaces or data interfaces for communicating with their decentralized peripherals, as shown in Fig. 2. These functionalities of the active component 1 in the PROFIBUS DP system comprise here the data transfer via a data interface 5, via input data areas (input data) 6 and output data areas (output data) 7, and also configuration, stages detection and diagnostics. The passive stations 2a, 2b, 2c and 2d each have an input area (input) and an output area (output). The passive component 2a comprises here an input area 8a and an output area 9a, the passive component 2b comprises an input area 8b and an output area 9b, the passive component 2c comprises an input area 8c and an output

area 9c and the passive component 2d comprises an input area 8d and an output area 9d. The passive components 2a, 2b, 2c and 2d are connected to the linear bus 4 via short spur lines, as is the active component 1. A large data memory is provided in the active component 1 and in it the input areas and output areas of the passive components are mirrored, that is to say are present in identical forms. For this purpose, the active component 1 updates its input areas 6 and output areas 7 cyclically with those of the passive components. The output areas 9a, 9b, 9c and 9d of the passive components contain here the data which is to be read out from the passive components to respectively decentralized peripherals, and the input areas 8a, 8b, 8c and 8d contain the data which is to be read from respective decentralized peripherals into the passive components. The input area 6 of the active component 1 contains data to be read out from the active component 1 to a decentralized peripheral, while the output area 7 of the active component 1 contains data which is to be read in from such a decentralized peripheral.

Fig. 3 is a schematic illustration of an active component 10 according to the present invention and of a passive component 11 according to the present invention. The active component 10 and the passive component 11 as illustrated in Fig. 3 can be integrated, for example, as an active component 1 or passive component 2a, 2b, 2c or 2d into the bus systems shown in Figs. 1 and 2.

The passive component 11 which is shown in Fig. 3 comprises a bus interface 21 for connecting the passive component 11 to a bus, such as for example a field bus, as has been described above. Furthermore, the passive component comprises a serial interface 22, for example a V.24 interface for serially reading in and reading out data into and out of a peripheral, such as for example a computer. Furthermore, a data memory 24 with an output area 25 for storing data which has been read

out via the bus interface 21 and is to be read in via the serial interface 22, and an input area 26 for storing data which has been read in via the serial interface 22 and is to be read out via the bus interface 21 is provided. The transmission and storage of data is controlled by a control device 23, an acknowledgement counter 27 for counting data packets which are read out via the serial interface 22, and a sequence counter 28 for counting data packets which are read in via the serial interface 22 being provided. The respective counting values serve as the status information with respect to the data packets stored in the output area 25 and input area 26. The acknowledgement counter 27 is embodied as part of the output area 25, while the sequence counter 28 is embodied as part of the input area 26. The data memory 24, which comprises the output area 25 and the input area 26, is, for example, a RAM (Random Access Memory). The control device 23 of the passive component 11 comprises a comparative device 29 to periodically compare the status information with corresponding status information of the active element 10, the control device 23 controlling the reading in and reading out of data via the output area 25 and the input area 26 on the basis of this periodic comparison. An optional buffer 30 for buffering data packets which are to be read out of the output area via the serial interface 22 is provided between the control device 23 and the serial interface 22. The buffer 30 is also used for buffering a data packet which is to be read into the input area 26 via the serial interface 22. The maximum size of the input area 26 and of the output area 25 of the passive component 11 can be set in a variable fashion, the data packets which are to be stored therein being able to have any desired size within the respectively set maximum size, as is explained in detail below.

The passive component 11 which is illustrated in Fig. 3 is connected to a correspondingly assigned active

element 10 via its bus interface 21 with a bus system, for example a field bus such as the PROFIBUS DP. The active element 10 correspondingly comprises a bus interface 13 with which it is connected to the bus system. In addition, the active component comprises a data memory 15, for example a RAM, with an output area 16 for storing data which is to be stored in the output area 25 of the passive element 11 and data which is to be read out via its serial interface 22, and an input area 17 of data which has been read out of the input area 26 of the passive component 11. As has been explained above, the data of the output area 16 of the active component 10 and of the output area 25 of the passive component 11 is cyclically mirrored and/or reconciled, like the data of the input area 17 of the active component 10 and the data of the input area 26 of the passive component 11. Here, the data of the output area 16 of the active component 10 is transferred in the output area 25 of the passive component 11, and the data of the input area 26 of the passive component 11 is transferred into the input area 17 of the active component 10. The active component 10 also comprises an optional serial interface 12 for serially reading data into the output area 16 and for serially reading data out of the input area 17. In addition, an acknowledgement counter 19 for counting data packets which have been read out via the serial interface 12, and a sequence counter 19 for counting data packets which have been read out via the serial interface 12 and a sequence counter 18 for counting data packets which have been read in via the serial interface 12 are provided, the counting values serving as the status information, which is used as the basis for the reading of data from the passive component 11 into the input area 17 via the bus interface 13 and for the reading of data out of the output area 18 to the passive component 11. The transmission of data is controlled here by the control device 14 which comprises a comparative device 20 to periodically compare the status information with corresponding

status information of the passive component 11, the control device 14 controlling the reading in and reading out of data on the basis of this periodical comparison. The acknowledgement counter 19 is embodied as part of the input area 17, and the sequence counter 18 is embodied as part of the output area 16.

Like the input area 26 and the output area 25 of the passive component 11, the input area 17 and the output area 16 of the active component 10 can also be set with respect to the maximum size, the data packets which are to be stored in them being able to have any desired size within the respectively set maximum size. The maximum size of the input areas 17 and 26 and of the output areas 16 and 25 is set by the active component 10 when the bus system is initialized. For this purpose, the active component 10 sets up the data communication to the passive component 11 in accordance with EN 50 170 and DIN 19 245 when operation is started and transmits a diagnostic message to the passive component 11. The passive component 11, i.e. the control device 23 receives the diagnostic message and signals the corresponding diagnostic parameters back to the active component 10, i.e. its control device 14. The control device 14 of the active component 10 then transmits the parameters to be set to the control device 23 of the passive component 11, as a result of which the latter is parameterized and configured. The setting of the parameters is correspondingly acknowledged by the passive element 11, in response to which the active component 10 transmits a configuration message to the passive component 11. From the configuration message, the passive component 11 detects the data area size for the input area 26 and the output area 25 and sets their sizes correspondingly. The sizes can be defined here in, for example, the limits 7 bytes to 244 bytes. The data area sizes which are set are then acknowledged by the passive component 11. During the further course of the operation, the data is cyclically updated in the input areas 17 and 26 and the

output areas 16 and 25. The abovementioned variable setting of the sizes of the output areas and of the input areas is supported in a corresponding way by corresponding algorithms in the control devices 14 and 23.

The passive component 11 according to the present invention is used exclusively for data communication between the bus system and one or more peripherals by means of the serial interface 22 and does not have require any further functions. However, it is also conceivable for the active component 11 according to the present invention to perform additional control or sensor functions in the bus system. The data which is to be read out of the output area 16 of the active component 10 to the output area 25 of the passive component 11 and then via the serial interface 22 of the passive component 11 generally includes data which is used to actuate passive components of the bus system which perform control, sensor and actuator functions and the like. The data which has been read via the serial interface 22 of the passive component into the input area 26 and from there into the input area 17 of the active component 11 includes data which comprises the messages of the corresponding peripheral, connected to the serial interface 22, to the active component 10, these messages being able to be used in turn for actuating other passive components of the bus system, for example.

In the passive component 11 according to the present invention, the data which is used within the bus system is thus converted into output data which is read out via the serial interface 22 to one or more decentralized peripherals, the serial interface 22 being able to be, for example, a V.24 or a RS 232 interface. On the other hand, the passive component 11 according to the present invention of one or more decentralized peripherals into the bus system converts data from serial data into data which has the data format necessary for the bus system.

In order to be able to transmit data between the bus system and one or more decentralized peripherals via the serial interface 22 of the passive component 11 or via the serial interface 12 of the active component 10, according to the present invention a further communications protocol, which is defined for example as in the following tables 1 and 2 is superimposed on the input areas 17 and 25 and the output areas 16 and 24. The serial interfaces 12 and 22 are given in this example as V.24 interfaces.

Table 1 presents the communications protocol for the output areas 16 and 24, that is to say the data transmission device from the active component to the passive component 11 for reading out the data via the serial interface 22 (V.24 interface) of the passive component 11.

Byte No.	**Designation**	**Function**
o-1	tx_seq	Sequence counter transmission of a V.24 telegram
o-2	rx_seq_ack	Acknowledgement counter for reception of a V.24 telegram
o-3	Command	Bit 0 0 no significance 1 reset of reception buffer DP slave before the
		new telegram is transmitted Bits 1..7 reserved
o-40	Reserved	00
o-5	rx_pref_len	Preset maximum byte number of a received telegram, if the value 00 is entered here the reception length is independently determined by the DP slave.
o-6	tx_len	Length data [byte] of telegram to be transmitted
o-7	Data 1	First octet to be transmitted via V.24
o-8	Data 2	Second octet to be transmitted via V.24
	Data...	...
o-(txlen +	Data [tx_len]	Last octet to be transmitted via V.24

6)		

Table 2 represents the communications protocol for the input areas 17 and 26, i.e. the data transmission device from the passive component 11 to the active component 10 for data packets (telegrams) which have been received via the serial interface 22 (V.24 interface) of the passive component 11.

Byte No.	Designation	Function
i-1	tx_seq_ack	Acknowledgement counter for transmit data V.24
i-2	rx_seq	Sequence counter for reception of a V.24 telegram
i-3	rx_tx_fail	Fault message DP-slave, for format see below.
i-4	Reserved	00
i-5	Reserved	00
i-6	rx_len	Length data [byte] of the received telegram, the maximum length given in the range o-5 is not exceeded (provided <>0).
i-7	Data 1	Received data 1
i-8	Data 2	Received data 2
:	:	:
i-rx len+6	Data [rx len]	Last octet received data

The reception buffer of the passive component 11 is the buffer 30 for buffering data packets which are to be read in or read out.

The following table 3 represents an example of the display of fault messages of the passive component 11 in the component i-3 of the communications protocol for the input areas.

Bit position	Significance
0	Reception buffer overflow
1	Reception error, frame error
2	parity error

3	Other reception errors
4	Reserved (=0)
5	Reserved (=0)
6	Reserved (=0)
7	Internal PROFIBUS DP-slave error

If there is error-free transmission, i.e. error-free reading in of data via the serial interface 22 into the reception memory or buffer (reception buffer) 30 into the input area 26, the byte i-3 is equal to 0. In the case of an error, i.e. if i-3 is unequal to 0, the received data are nevertheless to be read into the input area 26 via the buffer 30 and thus read into the input area 17 of the active component 11 by means of the cyclical reading out via the bus system.

The principle of the transmission mechanism for transmitting data packets data packets to be out of the output area 16 and into the output area 25 and via the serial interface 22 to one or more peripherals will be explained below. The transmission mechanism is based here on a comparison of the bytes o-1 and i-1 of the transmission protocols such as are illustrated, for example, in tables 1 and 2, in the comparator device 20 of the control device 14 of the active component 10 and the comparative device 29 of the control device 23 of the passive component 11. This means that the status or the current counter reading of the sequence counter 18 of the output area 16 and of the acknowledgement counter 27 of the output area 25 are compared. The two counter readings are each contained in byte o-1 and i-1. In principle, a data packet is not read out of the output area 16 of the active component 10 and into the output area 25 of the passive component 11 until the output area 25 is ready to receive this data packet, i.e. the output area 25 is empty. In order to speed up the reading of data packets out of the output area 16 of the active component 10 and into the output area 25 of the passive component 11, the data which is to be

read out of the output area 25 via the serial interface 22 is buffered in the buffer 30.

When the data is read out, the control device 14 of the active component 10 firstly checks the bytes o-1 and i-1 for identity. Given identity, data packets which are to be read out can be entered into the output memory 16 of the active component 10 and the data is then, in cyclical reading out, copied into the output area 25 of the passive component 11, from which it is then read out via the serial interface 22. Given non-identity between the bytes o-1 and i-1, the transmission mechanism is still occupied, i.e. the reading of data out of the output area 25 via the serial interface 22 is not yet terminated so that no new data packets are allowed to be entered into the output area 16 of the active component 10. Given identity between the two bytes, data packets which are to be read out are thus entered into the output area 16 of the active component 10 starting from the byte o-7. The overall length of the data is entered in the byte o-6. The byte o-1 is then incremented by the value +1, as a result of which the bytes o-1 and i-1 are differentiated. As long as this difference exists, no new data is allowed to be entered into the output area 16 of the active component 10.

The passive component 11, i.e. the comparator device 29 of the control device 23 also compares the bytes o-1 and i-1 and, when a difference is detected between these two bytes, it transmits output data from the output area 25 to the serial interface 22 via the buffer 30. When the reading-out operation from the output area 25 is terminated, the byte i-1 is incremented by the value +1, so that the byes i-1 and o-1 again have the same value, with the result that new data packets can be read into the output area 16 of the active component 10.

The reception mechanism for receiving data via the serial interface 22 of the passive component 11 is

equivalent. Here, the bytes i-2 and o-2 are each compared in the passive component 11 and in the active component 10. In principle, data packets are not read into the input area 26 of the passive component 11 via the serial interface 22 until the input area 17 of the active component 11 is ready to receive these data packets. The status of the input area 26 is detected via the sequence counter 28, while the status of the input area 17 is detected by the acknowledgement counter 19. The two bytes i-2 and o-2 (cf. tables 1 and 2) each represents the current status or counter reading of the sequence counter 28 or acknowledgement counter 19. When new data packets arrive at the serial interface 22 of the passive component 11, the comparator device 29 of the control device 23 checks the identity of the bytes i-2 and o-2. Given identity, the incoming data packets are allowed to be entered in the input area 26. Given non-identity, the incoming data packets must be buffered in the buffer 30. It is to be noted that the buffer can also be part of the memory 24, in particular if the latter is embodied as a RAM. When incoming data packets are stored in the input area 26, the received data is entered into the input area 26 starting from the byte i-7 (cf. table 2). The overall length of the received data packets is entered in the byte i-6 taking into account the length specification which is preset in the byte o-5. The byte i-2 is then incremented by +1 by the sequence counter 28, as a result of which the byte i-2 and o-2 are different.

The active component 10, i.e. comparator device 20 of the control device 14 detects the difference between the bytes o-2 and i-2 and reads the input data out of the input area 26 into the input area 17. Here, the error status can be obtained from the byte i-3. If the error status is not equal to 0, a serial error was detected when the data packets were received via the serial interface 22. The new data packets which have been read into the input area 17 of the active

component 10 are then read out of the input area 17 for further use, for example into other passive components of the bus system in order to actuate them. The release of the input area 17 is shown by the active component 10 in which the acknowledgement counter 19 increments the byte o-2 by the value +1, so that the bytes o-2 and i-2 have the same value again. The identity between i-2 and o-2, which is detected by the comparator device 29 in the passive component 11, indicates to the latter that new data packets can be entered into the input area 26.

The byte o-3 (command byte) shown in table 1 has no significance if it has the value 0. However, if the value 1 is set, the input area 26 of the passive component 11 is cleared in each case before new data packets which are to be read out from the output area 16 of the active component 10 via the serial interface 22. In this case, the control device 23 of the passive component 11 sets the byte i-2, i.e. the sequence counter 28, to the value of the byte o-2, i.e. the value of the sequence counter 18.

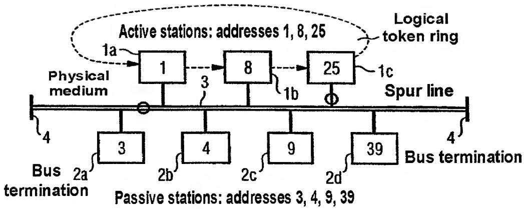
Furthermore, it is to be noted that it is not absolutely necessary to provide buffering of the data in the passive component 11 in the buffer 30 when data is read out via the serial interface 22. In this case, the buffering may, however, be useful because from the point of view of a passive component 11, the output area 25 is ready to receive again as quickly as possible so that new data packets can be transmitted from the output area 16 into the output area 25 of the passive component 11 by the active component 10. However, when data is read in via the serial interface 22 of the passive component 11, it is important to buffer the incoming data packets in the buffer 30 so that incoming data can be read in without delay. An overflow of the buffer 30 in this case is indicated in the output byte i-3 (cf. tables 2 and 3).

When the active component 10 fails, a watchdog which is prescribed by the corresponding standard, for example the PROFIBUS standard, must be detected by the passive component 11. Here, the last data packet of the active component 10 which was still completely received is read out of the output area 25 of the passive component 11 via the serial interface 22. When there is a network failure, no further data packets are received via the serial interface 22 of the passive component 11. Any data in the buffer 30 is rejected by the passive component. In the case of a network failure, or after such a failure, the entire input area of the passive component 11 is set to 0. As a result, a data packet which is received via the serial interface 22 and has the length 0 plus error status in the byte i-3 = 0, which corresponds to a synchronization message, is implicitly transmitted. If the passive component 11 can no longer be addressed via the bus system, owing, for example, to a network fault, the entire output area 16 of the active component 10 is set to 0. As a result, one or more data packets with the length 0 are implicitly transmitted to the passive component, i.e. a synchronous message.

When the passive component 11 is activated by the bus system and when it is integrated into the bus system, synchronization is necessary. Here, all the output data is set to zero by the active component 10 in the output area 16 with the exception of the byte o-3. The byte o-3 is set to 1 and thus indicates that the passive component 11 should reset its input area, i.e. to 0.

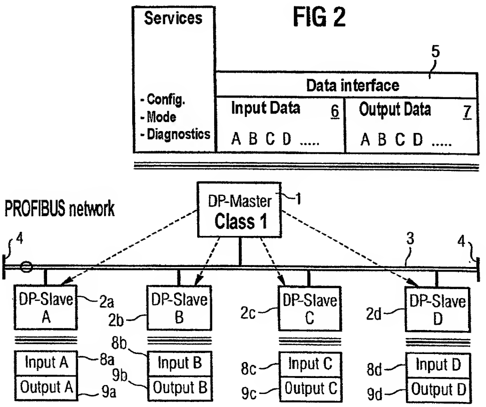
This means that the data in the input area 26 of the passive component 11 is cleared.

FIG 1



Active stations: addresses 1, 8, 25
Logical token ring
1a
1
8
25
1c
1b
3
Physical medium
Spur line
4
3
4
9
39
4
Bus termination
Bus termination
2a
2b
2c
2d
Passive stations: addresses 3, 4, 9, 39

FIG 2



Services
- Config.
- Mode
- Diagnostics
5
Data interface
Input Data 6
A B C D .....
Output Data 7
A B C D .....
PROFIBUS network
DP-Master Class 1
1
4
3
4
DP-Slave A
2a
DP-Slave B
2b
DP-Slave C
2c
DP-Slave D
2d
Input A
8a
Output A
9a
8b
Input B
9b
Output B
8c
Input C
9c
Output C
8d
Input D
9d
Output D

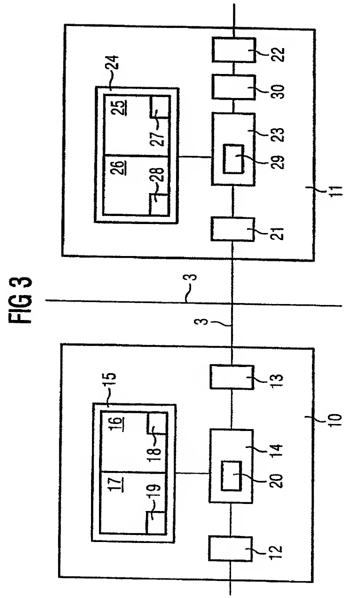


FIG 3

Declaration and Power of Attorney For Patent Application
Erklärung Für Patentanmeldungen Mit Vollmacht
German Language Declaration

Als nachstehend benannter Erfinder erkläre ich hiermit an Eides Statt:

dass mein Wohnsitz, meine Postanschrift, und meine Staatsangehörigkeit den im Nachstehenden nach meinem Namen aufgeführten Angaben entsprechen,

dass ich, nach bestem Wissen der ursprüngliche, erste und alleinige Erfinder (falls nachstehend nur ein Name angegeben ist) oder ein ursprünglicher, erster und Miterfinder (falls nachstehend mehrere Namen aufgeführt sind) des Gegenstandes bin, für den dieser Antrag gestellt wird und für den ein Patent beantragt wird für die Erfindung mit dem Titel:

Serielle Datenübertragung über ein Bussystem

deren Beschreibung

(zutreffendes ankreuzen)
☐ hier beigefügt ist.
☒ am 07.09.2000 als
PCT internationale Anmeldung
PCT Anmeldungsnummer PCT/DE00/03109
eingereicht wurde und am ______
abgeändert wurde (falls tatsächlich abgeändert).

Ich bestätige hiermit, dass ich den Inhalt der obigen Patentanmeldung einschliesslich der Ansprüche durchgesehen und verstanden habe, die eventuell durch einen Zusatzantrag wie oben erwähnt abgeändert wurde.

Ich erkenne meine Pflicht zur Offenbarung irgendwelcher Informationen, die für die Prüfung der vorliegenden Anmeldung in Einklang mit Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) von Wichtigkeit sind, an.

Ich beanspruche hiermit ausländische Prioritätsvorteile gemäss Abschnitt 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 119 aller unten angegebenen Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde, und habe auch alle Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde nachstehend gekennzeichnet, die ein Anmeldedatum haben, das vor dem Anmeldedatum der Anmeldung liegt, für die Priorität beansprucht wird.

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Serial data transmission via a bus system

the specification of which

(check one)
☐ is attached hereto.
☒ was filed on 07.09.2000 as
PCT international application
PCT Application No. PCT/DE00/03109
and was amended on ______
(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

German Language Declaration

Prior foreign appplications
Priorität beansprucht

Priority Claimed

19944041.7	DE	14.09.1999	☒ Yes / Ja	☐ No / Nein
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)		
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)	☐ Yes / Ja	☐ No / Nein
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)	☐ Yes / Ja	☐ No / Nein

Ich beanspruche hiermit gemäss Absatz 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 120, den Vorzug aller unten aufgeführten Anmeldungen und falls der Gegenstand aus jedem Anspruch dieser Anmeldung nicht in einer früheren amerikanischen Patentanmeldung laut dem ersten Paragraphen des Absatzes 35 der Zivilprozeßordnung der Vereinigten Staaten, Paragraph 122 offenbart ist, erkenne ich gemäss Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) meine Pflicht zur Offenbarung von Informationen an, die zwischen dem Anmeldedatum der früheren Anmeldung und dem nationalen oder PCT internationalen Anmeldedatum dieser Anmeldung bekannt geworden sind.

I hereby claim the benefit under Title 35. United States Code. §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §122, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occured between the filing date of the prior application and the national or PCT international filing date of this application.

PCT/DE00/03109	07.09.2000	anhängig	pending
(Application Serial No.) (Anmeldeseriennummer)	(Filing Date D, M, Y) (Anmeldedatum T, M, J)	(Status) (patentiert, anhängig, aufgegeben)	(Status) (patented, pending, abandoned)
(Application Serial No.) (Anmeldeseriennummer)	(Filing Date D,M,Y) (Anmeldedatum T, M; J)	(Status) (patentiert, anhängig, aufgeben)	(Status) (patented, pending, abandoned)

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German Language Declaration

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POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

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Unterschrift des Erfinders Datum 20.2.2002	Inventor's signature Date 20.2.2002
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Unterschrift des Erfinders Datum	Second Inventor's signature Date
Wohnsitz	Residence
Staatsangehörigkeit	Citizenship
Postanschrift	Post Office Address

(Bitte entsprechende Informationen und Unterschriften im Falle von dritten und weiteren Miterfindern angeben).

(Supply similar information and signature for third and subsequent joint inventors).

Form PTO-FB-240 (8-83)

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